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REPORT TITLE: **RF Broadband Amplifiers in CMOS Technology**

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I. INTRODUCTION

The increasing demand of high data rate transmissions and multi-standard multi-mode applications sets stringent requirements for RF transceivers and its components. A typical block diagram of most of the major circuit blocks that make up a typical superheterodyne communications transceiver is shown in Figure 1.1. Many aspects of this transceiver are common to all transceivers.

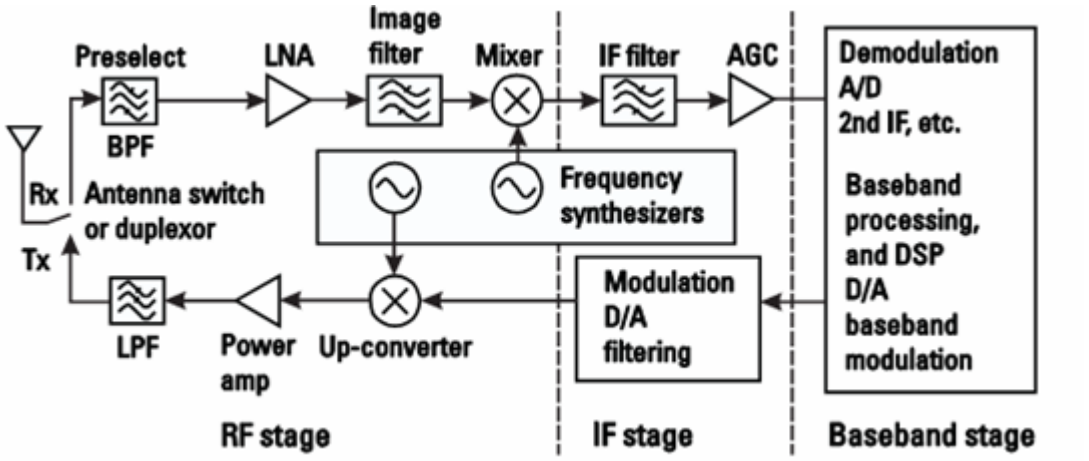

Figure 1.1 *Typical transceiver block diagram*

This transceiver has a transmit side (Tx) and a receive side (Rx), which are connected to the antenna through a duplexer that can be realized as a switch or a filter, depending on the communications standard being followed. The input preselection filter takes the broad spectrum of signals coming from the antenna and removes the signals not in the band of interest. This may be required to prevent overloading of the low-noise amplifier (LNA) by out-of-band signals. The LNA amplifies the input signal without adding much noise. The input signal can be very weak, so the first thing to do is strengthen the signal without corrupting it. As a result, noise added in later stages will be of less importance. The image filter that follows the LNA removes out-of-band signals and noise before the signal enters the mixer. The mixer translates the input RF signal down to the intermediate frequency, since filtering, as well as circuit design, becomes much easier at lower frequencies for a multitude of reasons. The other input to the mixer is the local oscillator (LO) signal provided by a voltage-controlled oscillator inside a frequency synthesizer. The desired output of the mixer will be the difference between the LO frequency and the RF frequency [4].

At the input of the radio there may be many different channels or frequency bands. The LO frequency is adjusted so that the desired RF channel or frequency band is mixed down to the same intermediate frequency (IF) in all cases. The IF stage then provides channel filtering at this one frequency to remove the unwanted channels. The IF stage provides further amplification and automatic gain control (AGC) to bring the signal to a specific amplitude level before the signal is

passed on to the back end of the receiver. It will ultimately be converted into bits that could represent, for example, voice, video, or data through the use of an analog-to-digital converter.

On the transmit side, the back-end digital signal is used to modulate the carrier in the IF stage. In the IF stage, there may be some filtering to remove unwanted signals generated by the baseband, and the signal may or may not be converted into an analog waveform before it is modulated onto the IF carrier. A mixer converts the modulated signal and IF carrier up to the desired RF frequency. A frequency synthesizer provides the other mixer input. Since the RF carrier and associated modulated data may have to be transmitted over large distances through lossy media (e.g. air, cable, and fiber), a power amplifier (PA) must be used to increase the signal power.

Power Amplifiers (PAs) are used in the transmit chain of communications devices, in order to amplify the signal to the desired power level. That power level is determined by the communications system - it must be high enough such that the amount of power that the receiver is able to sense (taking into account the losses in the communication medium) is adequate to recover the desired signal. For different applications, the order of magnitude of the transmitted power can vary greatly. For base-stations used in cellular systems, this can be on the order of tens to hundreds of watts. For satellite communications, this can be on the order of thousands of watts. For portable wireless communications devices, the peak transmitted power is often significantly less - it will vary from tens to hundreds of milliwatts in cordless systems to hundreds of milliwatts to a few watts in cellular systems. When speaking of the power output of these blocks, one common unit used is dBm, which is the output power in dB referenced to 1-mW. That is, the output power in dBm is given by Eq. 1.1

$$P_{dBm} = 10\log\frac{P}{0.001W}, \qquad \textit{(Eq. 1.1)}$$

where P is defined in watts. Thus 1-W is equivalent to 30dBm, 100-mW is equivalent to 20 dBm, etc.

In the cases where the power output is on the order of hundreds of milliwatts or more, the power that the PA needs to deliver to its load in itself is a large percentage of the total power consumed by the entire transmitter. The power that needs to be delivered will be taken from the source that powers the PA. In the case of a portable unit, this will be the battery. In essence, the PA converts the DC power from the battery into RF power delivered to the load. Unless that power conversion is lossless, which is possible only as an ideal abstraction, the PA itself will consume power, over and above what it delivers [5].

The measure of how much power a PA consumes in this conversion is one of the key performance parameters used to gauge PAs, especially those PAs used for portable applications. Because PAs in portable applications are driven from a source with a finite amount of available

energy, power consumed in the PA directly goes to reducing the battery life. This metric is known as the PAs efficiency, given by Eq. 1.2.

$$\eta = P_{out} / P_{dc} \qquad \textit{(Eq. 1.2)}$$

Since the PA is really converting the DC power of the supply into the RF power delivered to the load, the maximum efficiency is 1, or 100%. That is, if there is no power consumed in the PA - all the power from the supply is sent to the load - both the numerator and the denominator are the same. However, since this is only ideally possible, the biggest issue in PAs today is maximizing this metric.

The most common efficiency metric used, though, is the Power-Added Efficiency (PAE). PAE is the same as efficiency, but it takes the gain of the amplifier into account as follows:

$$\mathrm{PAE} = \frac{P_{\mathrm{out}} - P_{\mathrm{in}}}{P_{\mathrm{dc}}} = \frac{P_{\mathrm{out}} - P_{\mathrm{out}}/G}{P_{\mathrm{dc}}} = \eta\left(1 - \frac{1}{G}\right) \qquad \textit{(Eq. 1.3)}$$

where G is the power gain P_{out} / P_{in}. Thus, it can be seen in graph 1.2, that for high gain, power-added efficiency PAE is the same as dc-to-RF efficiency η.

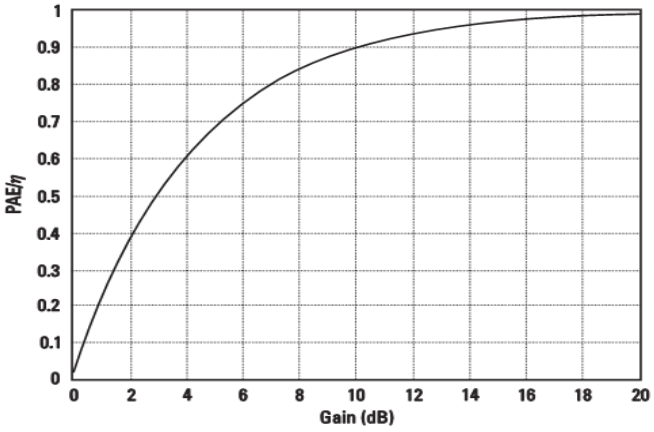

Figure 1.2 *Normalized power-added efficiency versus gain*

The millimeter-wave broadband amplifier is one of the key circuit blocks for high-speed optical communication systems. For wideband applications,wideband amplifiers were mostly fabricated in III-V or SiGe technologies to gain the better transistor performance. However, owing to the rapid scaling in the feature size, CMOS technology also becomes an excellent candidate for such applications. Not only with comparable f_T and f_{max}, but the MOS transistor also features high integration level, high yield, low power consumption, and low cost. Recent advances successfully demonstrated several wideband amplifiers using CMOS technologies.

II.BANDWIDTH EXTENSION TECHNIQUES

The design goal for broadband amplifiers is to maximize gain and bandwidth, and, for an acceptable linearity performance, to minimize power consumption.

Inductive peaking and distributed amplification are commonly used techniques for bandwidth extension. It is known that gain of a capacitively loaded amplifier rolls off as frequency increases because the capacitor's impedance diminishes. The introduction of an inductor in series with the load capacitor generates an impedance which increases with frequency (i.e. it introduces a zero). This nullifies the decrease in impedance of the capacitor and results in a constant impedance level over a broader frequency range as compared to the original RC network [11].

1. Inductive peaking

Inductive peaking can be achieved in a number of ways, depending on the placement of the coil:

1.1. Shunt peaking

Shunt peaking is achieved by placing an inductor in series with the load resistor (Fig. 2.1)

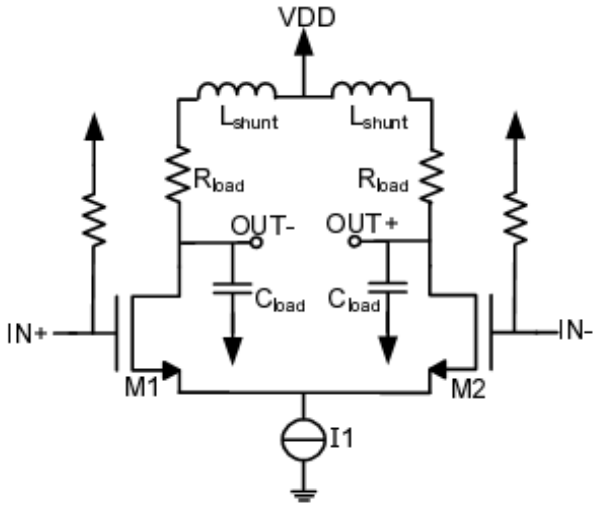

Figure 2.1 *Shunt peaking differential amplifier*

1.2. Series peaking

In series peaking the inductance is placed in series with the load capacitance. A combination of shunt and series peaking is also possible and offers increased bandwidth, than can be achieved by each system alone.

1.3. T-coil peaking

One of the best bandwidth extension methods is based on a combination of shunt and double series peaking and is called the T-coil peaking circuit. The circuit schematic of such a network is shown in fig. 2.2. The main characteristic of this circuit are the mutually coupled inductors (also referred as transformer) which form a letter 'T' if the mutual inductance is represented by a separate coil, hence the name T-coil is widely used [10].

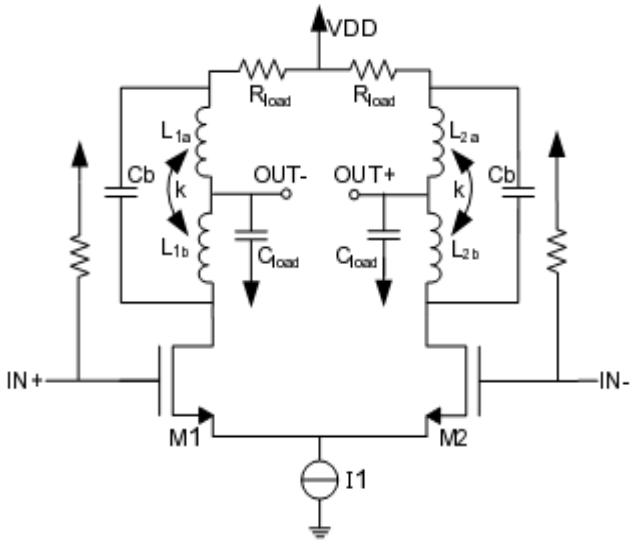

Figure 2.2 *T-coil peaking differential amplifier*

The coupling factor *k* between both halves of the coil (L1a,L1b or L2a,L2b) and the bridging capacitance Cb has a certain relationship, depending on the layout of network poles. For a general RLC circuit, to obtain constant input impedance at any frequency the relation R=√L/C must hold. However, this is true, only in a lossless circuit. In practice, owing to losses, the impedance is only constant up to a certain frequency, which, with careful design, can be high enough to work as a broadband amplifier.

The relation between different components of the T-coil amplifier are shown in equations 2.1 to 2.5. ζ is the damping factor and is chosen as 1/√2 for maximally flat response in the pass-band (also called Butterworth response).

$$\zeta = \frac{1}{4}\sqrt{\frac{C_{load}}{Cb}} \qquad \textbf{(Eq.2.1)}$$

L_M is the mutual inductance resulting from the coupling between the two halves of the coil L_{1a} and L_{1b}.

$$L_{1a} = L_{1b} = \frac{R_{load}{}^2 C_{load}}{2} \qquad \textbf{(Eq.2.2)}$$

$$L_M = \frac{R_{load}{}^2 C_{load}}{4}\left(\frac{1}{4\zeta^2} - 1\right) \qquad \textbf{(Eq.2.3)}$$

C_b, called the bridging capacitance is used to create parallel resonance and provides further bandwidth improvement. C_{load} consists of the output capacitance of the transistors as well as the bond-pad capacitance.

$$Cb = \frac{C_{load}}{16\zeta^2} = \frac{C_{load}}{4}\left(\frac{1-|k|}{1+|k|}\right) \qquad \textit{(Eq.2.4)}$$

$$w_n = \frac{1}{R_{load}\sqrt{Cb\ C_{load}}} \qquad \textit{(Eq.2.5)}$$

Theoretically, the T-coil peaking circuit improves the bandwidth by a factor of 2.83 as compared to a differential amplifier without inductive peaking.

1.4 Transformer peaking and matching

Transformers are attractive as they can simultaneously perform impedance transformation and differential-to-single-ended conversion. In a multistage design, they also provide easy DC biasing [4].

They can transform one resistance into another resistance depending on the ratio of the inductance of the primary and the secondary.

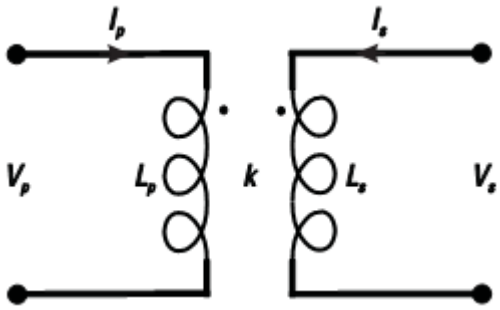

Figure 2.3 *A basic transformer structure*

Assuming that the transformer is ideal (that is,the coupling coefficient *k* is equal to 1, which means that the coupling of magnetic energy is perfect) and lossless, and

$$\boldsymbol{L_p = NL_s} \qquad \textit{(Eq. 2.6)}$$

then it can be shown from elementary physics that

$$\frac{V_p}{V_s} = \frac{I_s}{I_p} = \sqrt{N} \qquad \textit{(Eq. 2.7)}$$

Here we have defined *N* as the inductance ratio, but traditionally it is defined as a turns ratio. Since, in an integrated circuit, turns and inductance are not so easily related, this alternative definition is used.

Now if the secondary is loaded with impedance R_s, then the impedance seen in parallel on the primary side R_p will be

$$R_p = \frac{V_p}{I_p} = \frac{V_s\sqrt{N}}{\frac{I_s}{\sqrt{N}}} = \frac{V_s}{I_s}N = R_s N$$

(Eq. 2.8)

Thus, the impedance on the primary and secondary are related by the inductance ratio. Therefore, placing a transformer in a circuit provides the opportunity to transform one impedance into another. However, the above expressions are only valid for an ideal transformer where $k = 1$. Also, if the resistor is placed in series with the transformer rather than in parallel with it, then the resistor and inductor will form a voltage divider, modifying the impedance transformation. In order to prevent the voltage divider from being a problem, the transformer must be tuned or resonated with a capacitor so that it provides an open circuit at a particular frequency at which the match is being performed. Thus, there is a trade-off in a real transformer between near-ideal behavior and bandwidth. Of course, the losses in the winding and substrate cannot be avoided.

Unlike the previous case where the transformer was assumed to be ideal, in a real transformer there are losses. Since there is inductance in the primary and secondary, this must be resonated out if the circuit is to be matched to a real impedance. To do a more accurate analysis, we start with the equivalent model for the transformer loaded on the secondary with resistance R_L, as shown in the Eq.2.6.

Next, we find the equivalent admittance looking into the primary. Through circuit analysis, it can be shown that

$$Y_{\text{in}} = \frac{-R_L\omega^2(L_sL_p - M^2) - j\omega^3(L_sL_p - M^2) - j\omega R_L^2 L_p + \omega^2 L_s L_p R_L}{\omega^4(L_sL_p - M^2)^2 + \omega^2 R_s^2 L_p^2}$$

(Eq. 2.9)

Taking the imaginary part of this expression, the inductance seen looking into the primary $L_{eff\text{-}p}$ can be found, making use of the equivalent models of a transformer (Fig. 2.4) to express the results in terms of the coupling coefficient k:

$$L_{\text{eff-}p} = \frac{\omega^2 L_s^2 L_p(1-k^2)^2 + R_L^2 L_p}{\omega^2 L_s^2(1-k^2) + R_L^2}$$

(Eq. 2.10)

When $k = 1$ or 0, then the inductance is simply L_p. When k has a value between these two limits, then the inductance will be reduced slightly from this value, depending on circuit values. Thus, a transformer can be made to resonate and have a zero reactive component at a particular frequency using a capacitor on either the primary C_p or secondary C_s.

$$\omega_o = \frac{1}{\sqrt{L_{\text{eff-}p}\, C_p}} = \frac{1}{\sqrt{L_{\text{eff-}s}\, C_s}} \qquad \textit{(Eq. 2.11)}$$

where $L_{eff\text{-}s}$ is the inductance seen looking into its secondary.

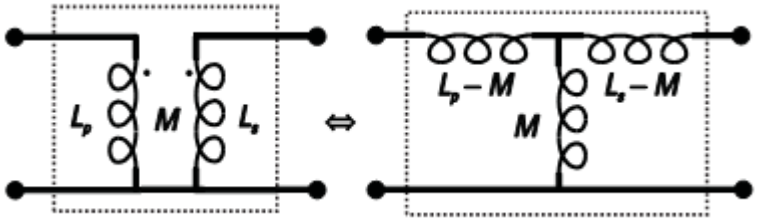

Figure 2.4 *Two equivalent models for a transformer*

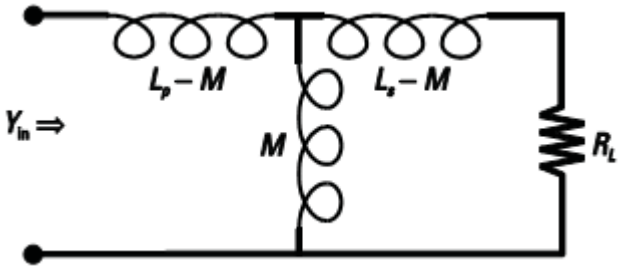

Figure 2.5 *Real transformer used to transform one resistance into another*

The exact resistance transformation can also be extracted and is given by

$$R_{\text{eff}} = \frac{R_L^2 L_p - \omega^2 L_s^2 L_p (1 - k^2)^2}{R_L L_s k^2} \qquad \textit{(Eq. 2.12)}$$

If $k = 1$, then $R_{eff} = R_L.N$ and goes to infinity as k goes to zero.

1.5. Comparison between various peaking techniques, applied to a five stage Common Source design

A comparison between the simulated results achieved by applying various peaking techniques to a basic configuration of a five-stage CS design (Fig. 2.6) is shown in graph 2.7.

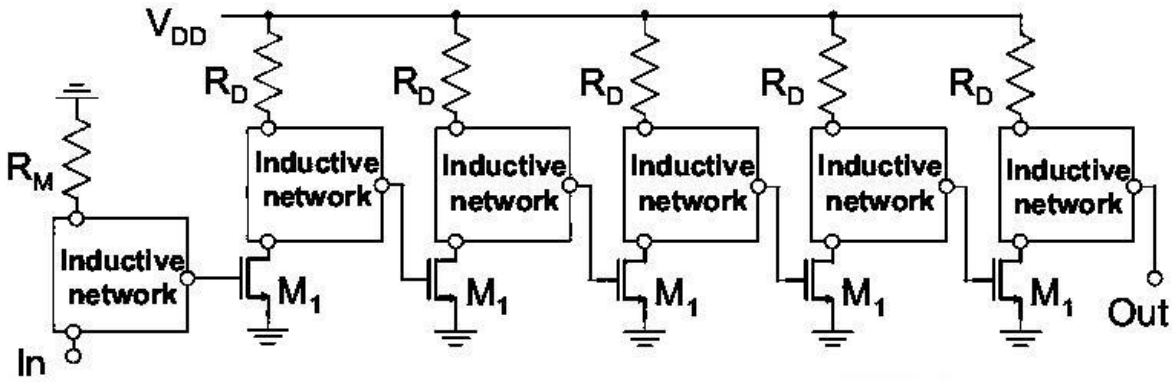

Figure 2.6 *A basic five-stage CS structure*

Based on the foundry provided BSIM model and the ideal inductive components, these designs present a similar low-frequency gain but with an obvious bandwidth difference. Without using any inductive peaking techniques, the low-frequency gain is 10.3 dB and the circuit bandwidth is only 7.0 GHz, as shown in the diagram 2.7, curve *A* [2].

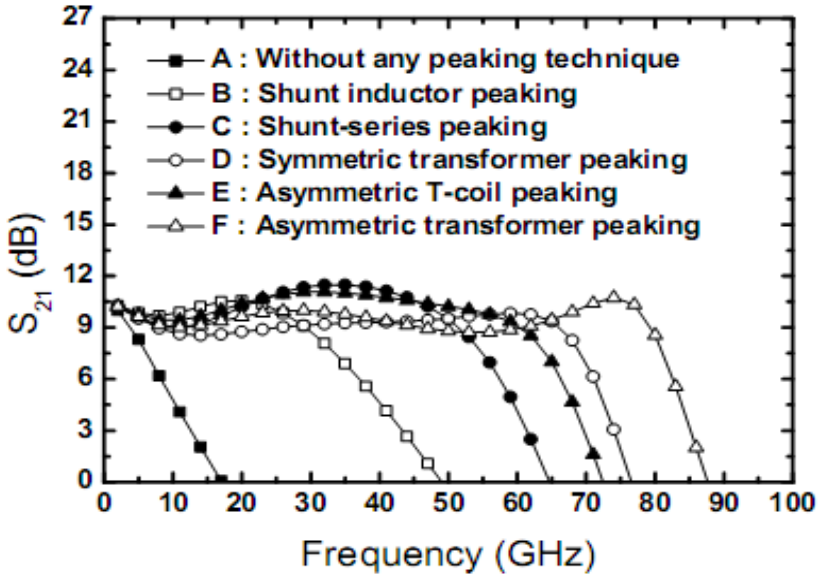

Figure 2.7 *Simulated frequency responses with different inductive peaking techniques*

The most straightforward wideband technique is the shunt inductor peaking. By placing an inductor in series with the load resistor R_D, the drain capacitance C_d and the gate capacitance C_g of the next stage can be canceled out by the shunt *LC* resonance. As a result, the bandwidth is increased up to 34.1 GHz, as shown by curve *B*. For curve *C*, one more inductor is connected in series between the drain and the gate of the next stage to form the shunt-series peaking, and the bandwidth can be further enhanced to 55.5 GHz.

As shown by curve *D*, the symmetric transformer peaking technique is employed, which has a positive *k* and the identical primary coil L_p and secondary coil L_S inductances in each transformer. Similar to the proposed asymmetric transformer peaking design, one zero and two pairs of complex poles are also introduced. However, the bandwidth is enhanced to only 69.7 GHz since the identical L_p and L_S resulting in lower pole / zero frequencies. The result of a recently published peaking technique, asymmetric T-coil peaking, is shown by curve *E*, where *k* is negative and L_p and L_S are different. As can be seen, the obtained bandwidth of the amplifier with asymmetric T-coil peaking is 64.7GHz. With the asymmetric T-coil design, the unequaled inductances can accommodate the unequaled parasitic loading capacitances for an enhanced bandwidth extension. However, with a negative *k*, the impedance looking into L_p is large, which reduces the current $g_m v_{gs}$ flowing into the gate capacitance C_g and handicaps the bandwidth enhancement.

By using asymmetric transformer peaking with a positive *k*, a simulated circuit bandwidth of 81.4 GHz can be achieved, as shown by curve *F*.

2. Distributed amplifiers (DA) and cascaded single-stage distributed amplifiers (CSSDA)

The distributed amplifier (DA) architecture is well-known and widely used in instruments, electronic warfare, optical communications, broadband commercial and military radio systems. In general, the traveling-wave architectures can be classified into conventional distributed amplifier (DA) and cascaded single-stage distributed amplifier (CSSDA). The basic concept of a DA is to take a number of transistors and form artificial transmission lines using inductors connected between successive gates, on the input, and drains, on the output. The architecture and equivalent circuit of ideal lossless DA and CSSDA are shown on figures 2.8 and 2.9

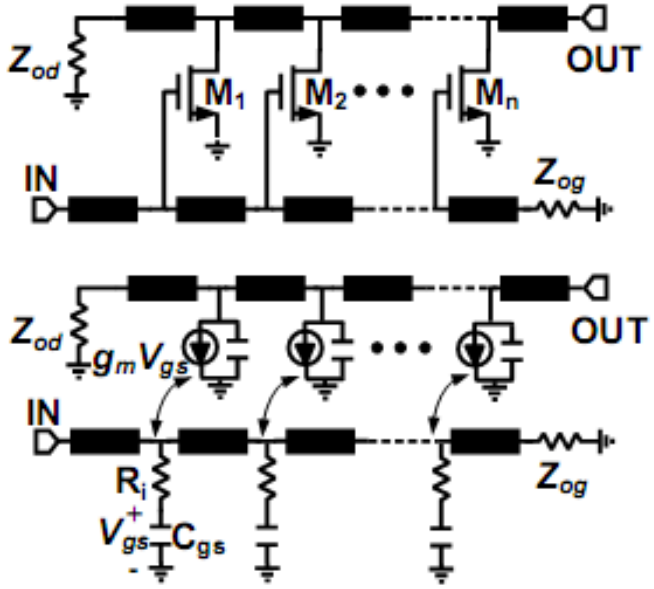

Figure 2.8 *Architecture and equivalent circuit of DA*

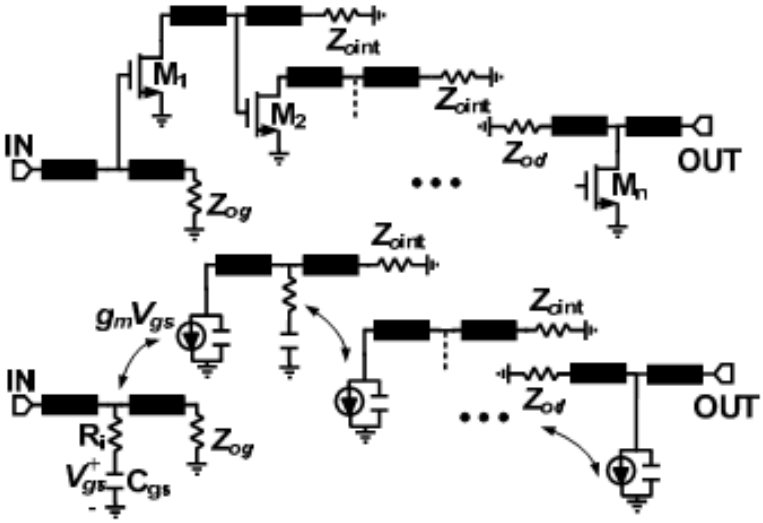

Figure 2.9 *Architecture and equivalent circuit of CSSDA*

The equation for available power gain of ideal lossless DA is:

$$G_{av} \cong \frac{n^2 g_m{}^2 Z_{od} Z_{og}}{4} \qquad \textit{(Eq. 2.13)}$$

While the equation for available power gains of ideal lossless CSSDA is:

$$G_{av} \cong \frac{g_m{}^{2n} Z_{o\,in}{}^{2(n-1)} Z_{od} Z_{og}}{4} \qquad \textit{(Eq. 2.14)}$$

The disadvantages of the DA topology are the relatively large power consumption and chip area due to the long length and the associated loss of the transmission lines.

CSSDA has a potential of higher gain-bandwidth performance than DA. The gain can be increased easily by increasing the number of devices and CSSDA is not restricted to an optimum number of active devices. With CSSDA configuration a flat gain, good input-output isolation, good input-output return loss is achievable for broadbandwidth performance. The CSSDA is simple to implement in practice. Another advantage of CSSDA is that it is easy for matching, as it only requires matching of the first stage to the 50Ω source impedance and the last stage to the 50Ω load impedance. The interstages do not require 50Ω matching. Therefore the device can be optimized to boost the overall available power gain of the amplifier [6].

The main disadvantage of CSSDA is that its output power is limited by the device size of the last stage. Using larger devices, the output power can be increased, however, larger devices have larger parasitic capacitance and thus this approach limits the bandwidth.

III. RF BROADBAND AMPLIFIERS IN CMOS TECHNOLOGY

The standard CMOS technology can offer gain, bandwidth, and power performances comparable to advanced compound semiconductor technologies.

1. Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology

The standard CMOS technology can offer gain, bandwidth, and power performances comparable to advanced compound semiconductor technologies.

The distributed amplifier (DA) architecture is well-known and widely used in instruments, electronic warfare, optical communications, and broadband commercial and military radio systems. A record DA in SOI CMOS process is demonstrated in with high GBW using devices with f_T and f_{max} of 196 and 230GHz. The challenges of CMOS DA design at high frequency include conductive Si-substrate and topology limitations. A circuit topology with coplanar waveguides (CPWs) to reduce substrate loss is demonstrated in [3] using a standard 90nm 1P9M CMOS technology, with a f_T of 160GHz and an f_{max} of 142GHz. This circuit indicates that standard CMOS technology is also promising for broadband applications up to 70GHz with good output power performance.

Although CSSDA has a potential of higher gain-bandwidth performance than DA, its output power is limited by the device size of the last stage. Using larger devices, the output power can be increased, however, larger devices have larger parasitic capacitance and thus this approach limits the bandwidth. In order to overcome this bottleneck, a new design concept to improve CSSDA performance is proposed. The single cells of CSSDA are replaced by distributed cells to construct a broadband CMSDA. As in CSSDA, the CMSDA can have the following features:

- The characteristic impedance of the input and output artificial transmission lines are matched to the 50Ω environment;
- The inter-stage impedance can be optimized to boost the overall gain performance.

The proposed in [3] CMOS CMSDA, which is a cascaded two-stage distributed amplifier, and each stage is composed of two gain cells is shown on figure 3.1.

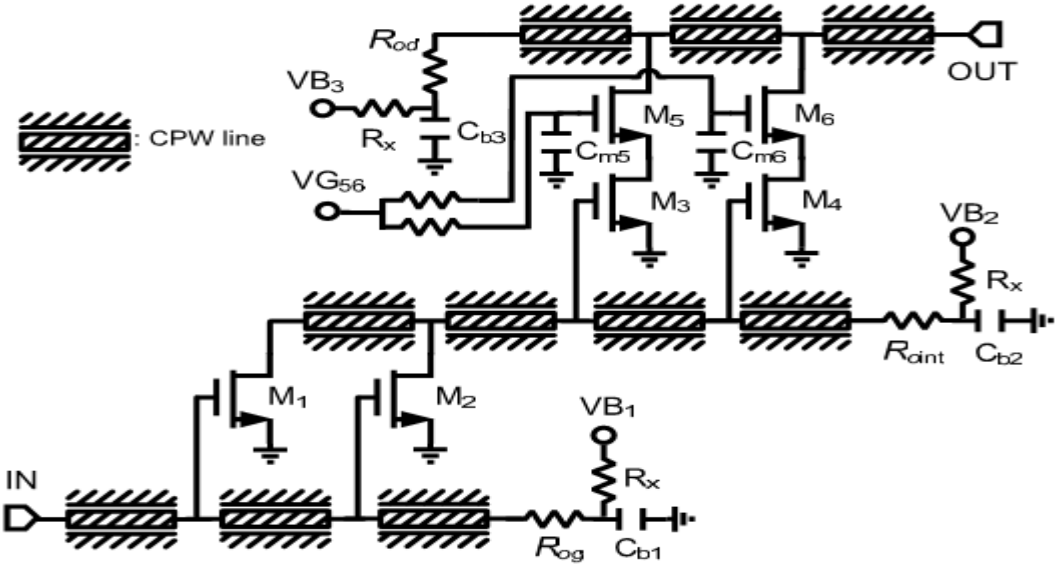

Figure 3.1 *CMOS CMSDA*

Each gain cell of the first stage is a common-source transistor connected with CPW lines, and the second (output) stage consists of two broadband cascode architectures, providing high gain-bandwidth performance. The input and output CPWs are terminated by 50Ω polysilicon resistors R_{og} and R_{od} in series with bypass capacitors C_{b1} and C_{b2}, respectively. These capacitors with the inductance of supply line introduce a low-frequency pole, and hence, the resistor R_x is used to prevent low-frequency instability. The output parasitics of M_1 and M_2 are coupled into the inter-stage transmission lines, which also drive the output line through $M_{3\text{-}6}$. The gates of cascode devices (M_5, M_6) are bypassed using 1pF capacitors ($C_{m5,}$ C_{m6}) and for stability consideration are biased separately through high-resistivity polysilicon resistors. The inductances of the artificial transmission lines are all realized by CPW with suppression of coupled-slot-line mode using underground passes.

S-parameters are measured via on-wafer probing, as shown in figure 3.2.

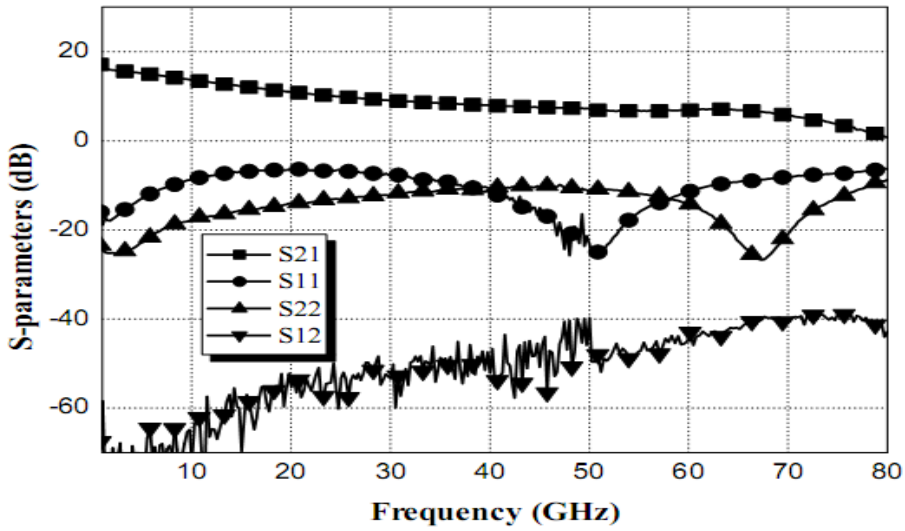

Figure 3.2 *Measured S-parameters of the CMSDA*

The measured gain is better than 7dB and the 3dB cut-off frequency is at 74GHz with input and output return losses of better than 7dB and 10dB. Reverse power gain (*S12*) is lower than –40dB due to the good isolation of the circuit architecture and the cascode gain cells. The total power consumption is 122mW. The measured results of the P_{1dB} and IMD3 are shown on figure 3.3.

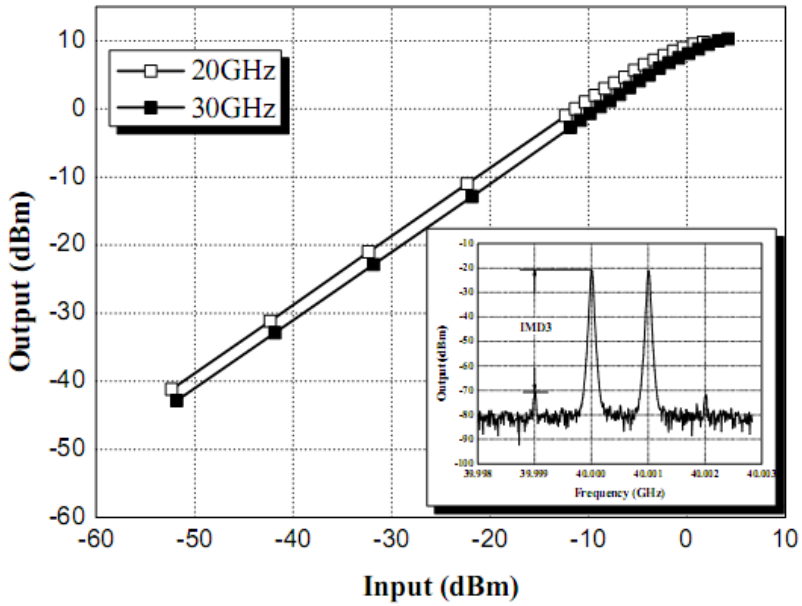

Figure 3.3 *Measured P_{1dB} and IMD3*

The P_{1dB} is measured at 20 and 30GHz with a 10dBm output power. The IMD3 is measured at 40GHz. For a –16.2dBm input, IMD3 is 51dB below the carrier which is equivalent to a +9.3dBm IIP3. This MMIC features an average NF of 6.4dB between 1 to 25GHz.

The die micrograph of the fabricated chip, proposed in [3] is shown in figure 3.4. The die size is 0.9x0.8mm^2 including all testing pads and dummy metal.

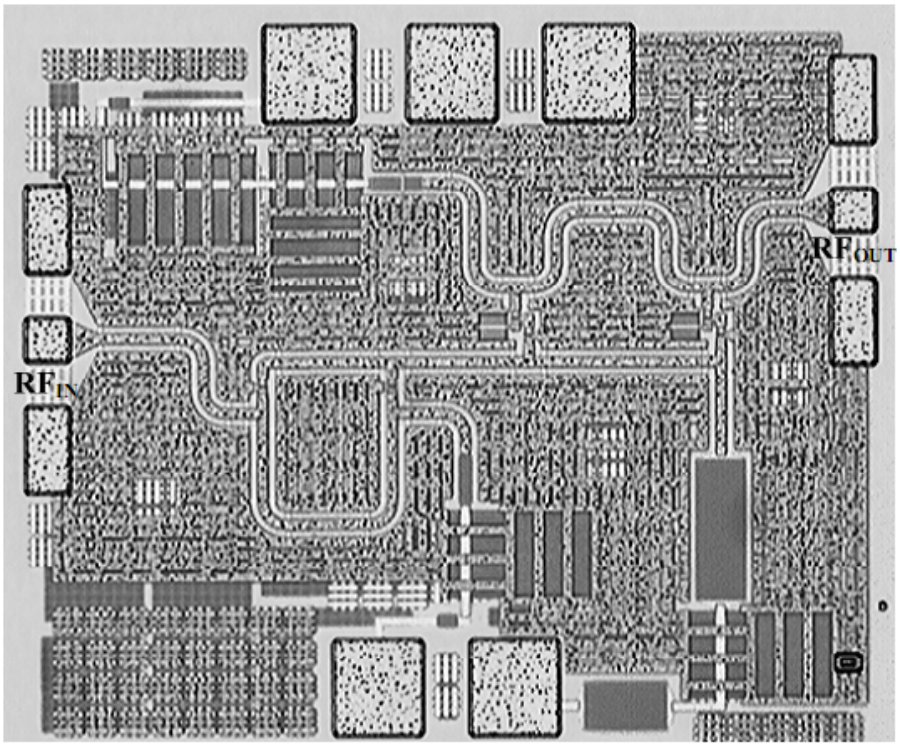

Figure 3.4 *Chip micrograph*

The proposed miniature MMIC can provide good output power at millimeter-wave frequency, has high linearity and gain-bandwidth performance, and represents the state-of-the-art broadband amplifier in standard CMOS technology.

2. A 60GHz Transformer-Coupled Wideband PA in 90nm CMOS

Most of the mm-wave PAs reported use bulky transmission lines, which leads to the increasing silicon area and incurring higher substrate losses. This disadvantage is avoided in the examined fully integrated 60GHz transformer-coupled two-stage differential power amplifier with single-ended input and output in 90nm digital CMOS with no RF process options. On-chip transformers for a 60GHz PA are used as an integrated CMOS solution. Operating from a 1V supply, it achieves a 1dB compressed output power of +9dBm and saturated power of +12.3dBm. The chip occupies an area of only 660x380μm^2 by taking advantage of the extensive use of small transformers. Transformers are attractive as they can simultaneously perform impedance transformation and differential-to-single-ended conversion. In a multistage design, they also provide easy DC biasing. In this design, a 1:1 vertical transformer is built with two coupled loop inductors. The diameter of the loop inductors is an important design metric. For very small sizes, the impedance of the shunt magnetizing inductance becomes too small and most of the signal current is lost through it. A large transformer results in higher substrate losses and an increased series leakage inductance which also reduces the signal transfer to the secondary winding.

Transformers with different diameters and trace widths have been implemented with the top

two metal layers.

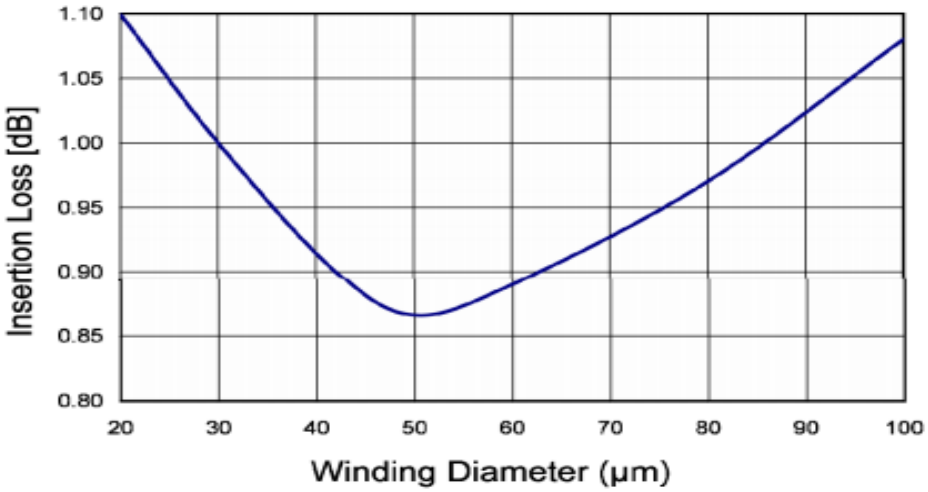

Figure 3.5 *Simulated minimum insertion loss of 60 GHz transformers as a function of diameter of the windings*

The diagram shows the simulated minimum insertion loss of 60GHz transformers, clearly indicating how the size can be optimized. It shows the measured insertion loss versus frequency of a vertical transformer with a 42µm diameter and 8µm trace width. At 60GHz, the loss is below 0.9dB, showing the potential of transformers at these frequencies. The measured S_{21} shows the broadband nature of transformers, with 3dB bandwidth close to 30GHz.

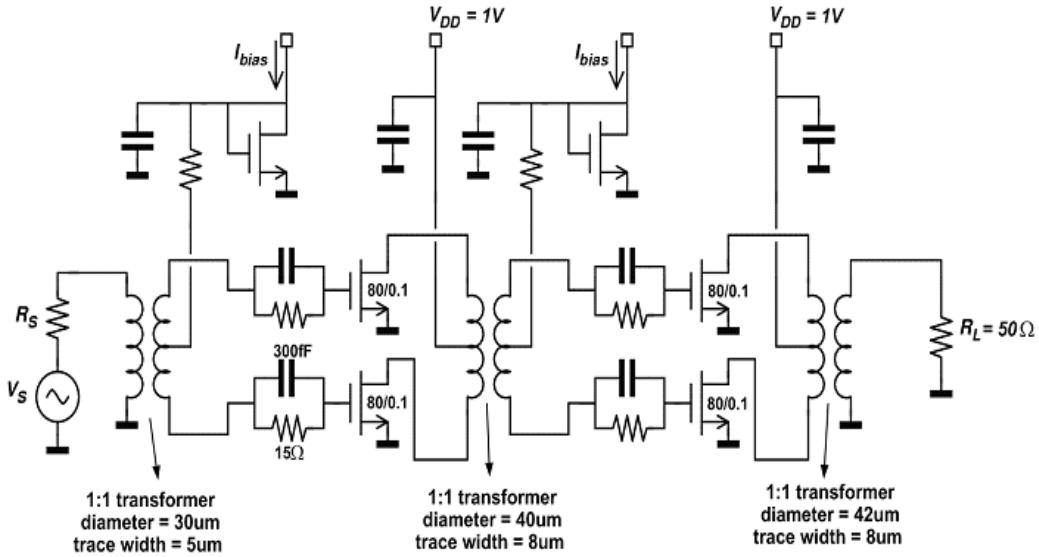

Figure 3.6 *Schematics of the two stage differential transformer-coupled power amplifier*

The design of the PA is a simultaneous optimization of output power, power gain and efficiency while ensuring unconditional stability over all frequencies. The implemented circuit is shown on figure 3.6. It consists of two differential amplifier stages and optimized transformers for input, inter-stage, output matching and differential-to-single-ended conversion. The use of transformers eliminates the need for AC coupling capacitors and RF chokes while differential

operation reduces the amount of bypass capacitance needed. A difference in mm-wave PA design versus lower frequencies is a pronounced limitation on the maximum device width. Choosing the size of the output NMOS transistor is a compromise between maximum stable gain (MSG) and maximum output power. For high gain, the width of a finger needs to be small enough. On the other side, for high output power, the total width needs to be large. This means that a large number of fingers need to be placed in parallel; the connections to all these fingers introduce lossy parasitics, reducing gain and efficiency [1].

In order to simultaneously optimize the PA and transformers, the following systematic design algorithm is used:

- An appropriate NMOS device size (W=1μm, W=80μm in our design) and bias current (22mA) are selected, ensuring that the device is biased near peak f_t current density (0.3mA/μm). The contours for constant 1dB compressed output power and power gain (Gp) are then plotted on a Smith chart and an optimum drain load impedance (Z_{opt}) is chosen (Figure 3.7). Simultaneously, it is important to plot the load stability circle to ensure that Z_{opt} is far from it;

- The diameter and trace width of the output transformer are optimized to efficiently transform the 50Ω load impedance to the chosen value Z_{opt} for each single-ended stage. The pad parasitics are taken into account and pad capacitance is used to tune the transformer secondary inductance. No additional tuning capacitors are used;

- Besides presenting Z_{opt}, the transformer should also have low insertion loss. Minimum insertion loss of the transformer, which assumes conjugate matching, is not the appropriate metric here. It is a good measure for the purpose of comparison between different transformers, but the more appropriate metric is the power gain (Gp) of the transformer (Figure 3.8), which takes into account the fact that the load impedance is fixed to 50Ω. The design goal is transformer Gp to be maximized, while simultaneously ensuring its input impedance is close to Z_{opt}.

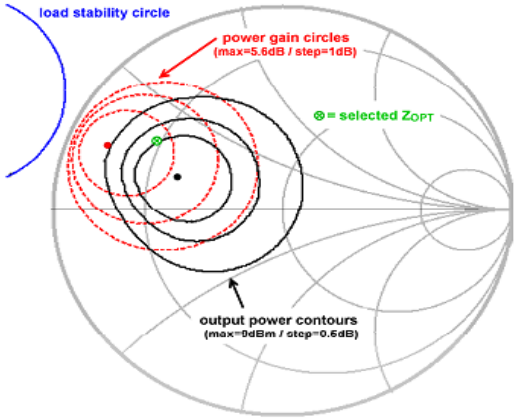

Figure 3.7 *Load stability circle, power gain circles and 1 dB compressed output power contours at 60 GHz for a single 80 μm transistor with input stabilizing network*

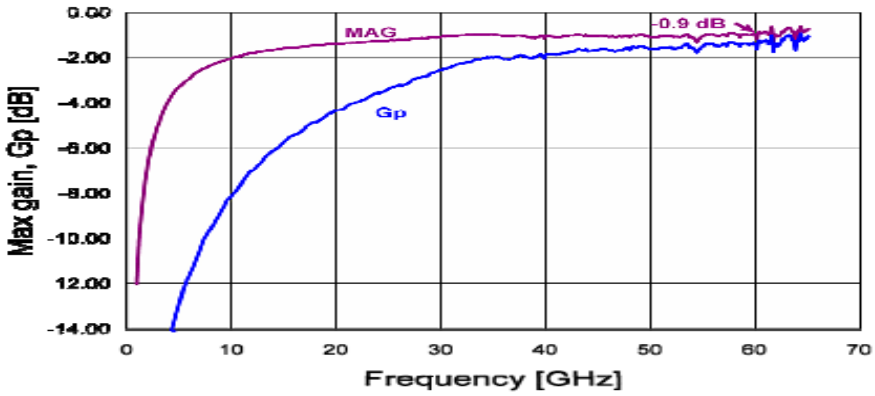

Figure 3.8 *Maximum available gain (MAG) and power gain (G_p for a 50 Ω load) of a 1:1 vertical transformer with an inner diameter of 42 µm and trace width of 8 µm*

A similar procedure is adopted for the design of the inter-stage and input stage transformers. The driver is designed to avoid compression when the output starts to saturate.

The circuit is prone to instability in the 20÷40GHz band, since the transistor gain increases but the losses of the transformer do not go up significantly. But stability is a prime consideration in mm-wave PAs, and then an RC stabilization network is added at the gate of each transistor (fig.3.8). This network is sized to ensure resistive loss below 40GHz, without significantly affecting the power gain at 60GHz. The losses also improve low-frequency common mode stability. The gate bias lines through the transformer center taps have been adequately de-qued to quench common-mode oscillations. Transformers also help decouple the common-mode behavior of driver and output stages and make output-stage common-mode stability VSWR independent.

The prototype PA is fabricated in a 90nm 1P7M digital CMOS process. The measured S-parameters are shown in figure 3.9.

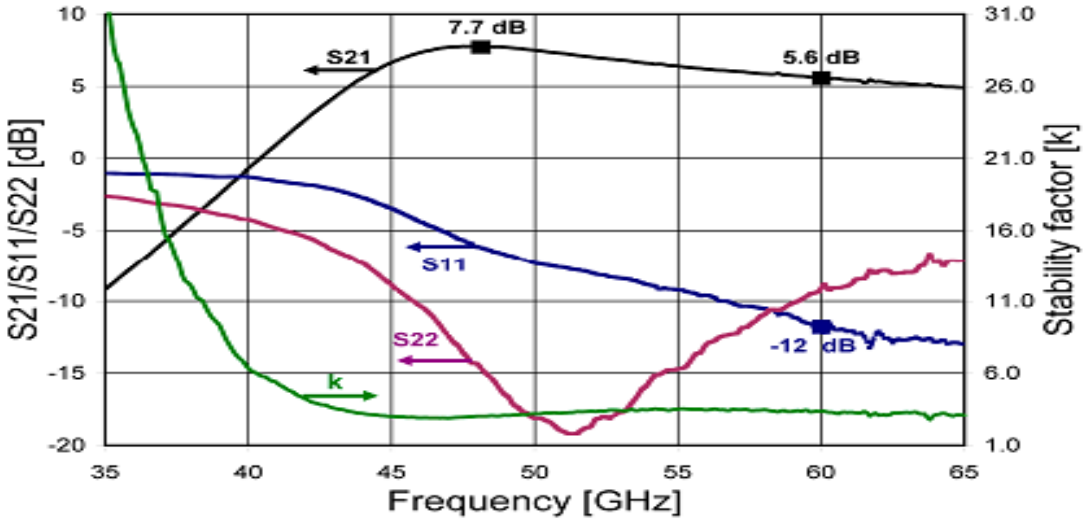

Figure 3.9 *Measured S-parameters and k-factor of the PA*

At a supply voltage of 1V, S21 at 60GHz is 5.6dB and has a peak value of 7.7dB at 48GHz. The 3dB bandwidth of the amplifier exceeds 22GHz (43 to 65GHz; upper point limited by VNA). The

input match is better than −8dB from 50 to 65GHz. The amplifier is unconditionally stable at all frequencies as indicated by the measured stability factor (*k*) in figure 3.10.

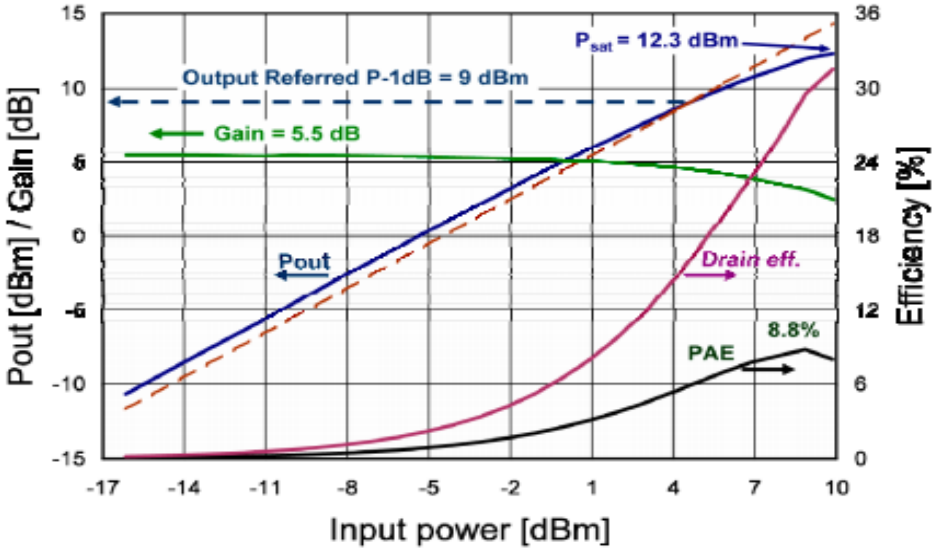

Figure 3.10 *Large Signal output power, gain and efficiency measurements*

Using a 1V supply, the measured 1dB compressed output power is +9dBm and saturated output power is +12.3dBm, which are the highest reported for a 60GHz CMOS PA. This power is also comparable to some SiGe amplifiers operating from higher supply voltages. The measured peak drain efficiency is 32% and peak PAE, including DC power consumption of the driver stage, is 8.8%. The PAE can be improved by using a smaller size cascode driver stage. The measured P_{1dB} a peak value of +9.7dBm at 50GHz.

The small die size of 660x380μm^2, including probe pads, clearly demonstrates the area benefit of using transformers at mm-wave frequencies. The chip micrograph is shown in figure 3.11.

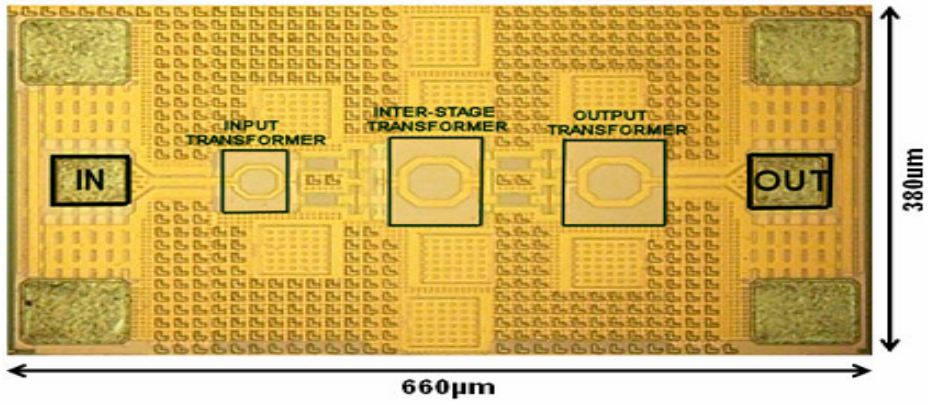

Figure 3.11 *Chip micrograph*

3. A Transformer-Peaking Broadband Amplifier in 0.13-μm CMOS Technology

Two design approaches are commonly adopted for wideband amplifiers, namely, the distributed amplifier (DA) topology and the inductive peaking technique. The disadvantages of the

DA topology are the relatively large power consumption and chip area due to the long length and the associated loss of the transmission lines. On the other hand, the circuit area is mainly limited by the size of the inductive components if using the inductive peaking technique.

In this part, a 0.13-µm CMOS broadband amplifier is realized using the proposed in Chapter II, p.1.4 asymmetric transformer peaking technique in a simple cascaded common-source (CS) configuration. By an effective frequency peaking design using transformers, this amplifier achieves a bandwidth of 70.6 GHz under a low power consumption of 79.5 mW. The miniaturized transformers using the interconnect layers in the CMOS process result in an overall circuit core area of only ~ 0.05 mm^2 [2].

The circuit topology of the proposed broadband amplifier is shown in the figure 3.12.

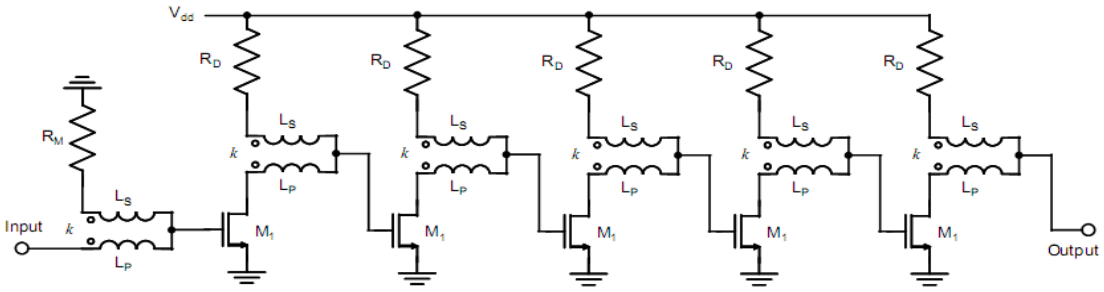

Figure 3.12 *Circuit topology of the CMOS broadband amplifier*

Transformers with a positive coupling coefficient *k* are employed to extend the operation frequency and also for input / output impedance matching. One zero and two pairs of complex conjugate poles are introduced by the transformers at different frequencies to enhance the circuit bandwidth. A shunt resistor R_M is placed at the input node together with the input transformer for impedance matching. A similar topology is also employed in the last stage for output matching using the drain bias resistor R_D. For low voltage and low power operation, the simple CS design is adopted instead of the typically used cascode topology for RF applications. As shown in the fig. 3.12, five stages are cascaded to provide a high gain amplification while still maintaining an overall low power consumption.

The broadband amplifier was fabricated in a standard 1P8M 0.13-µm CMOS process. The chip area including the DC and RF probing pads is 0.66x0.59 mm^2, while the core area is only 0.48x0.11 mm^2 (~ 0.05 mm^2), as shown in figure 3.13.

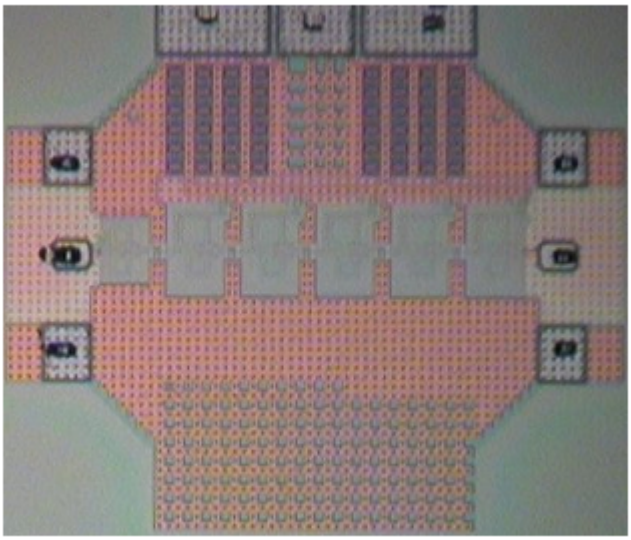

Figure 3.13 *Chip photograph (Chip area: 0.66 x 0.59 mm^2)*

The on-wafer S-parameters measurement was performed from 2 GHz to 100 GHz. The measured *S21* at low frequencies is 10.3 dB and the circuit bandwidth is 70.6 GHz under a power consumption P_{DC} of 79.5 mW, as shown in figure 3.14.

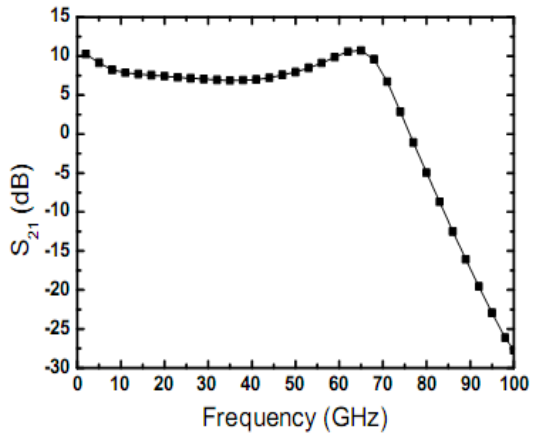

Figure 3.14 *Measured S21 of the proposed broadband amplifier*

The measured maximum *S11* and *S22* are -6.1 dB and -10.8 dB within the circuit bandwidth, as shown in diagram 3.15.

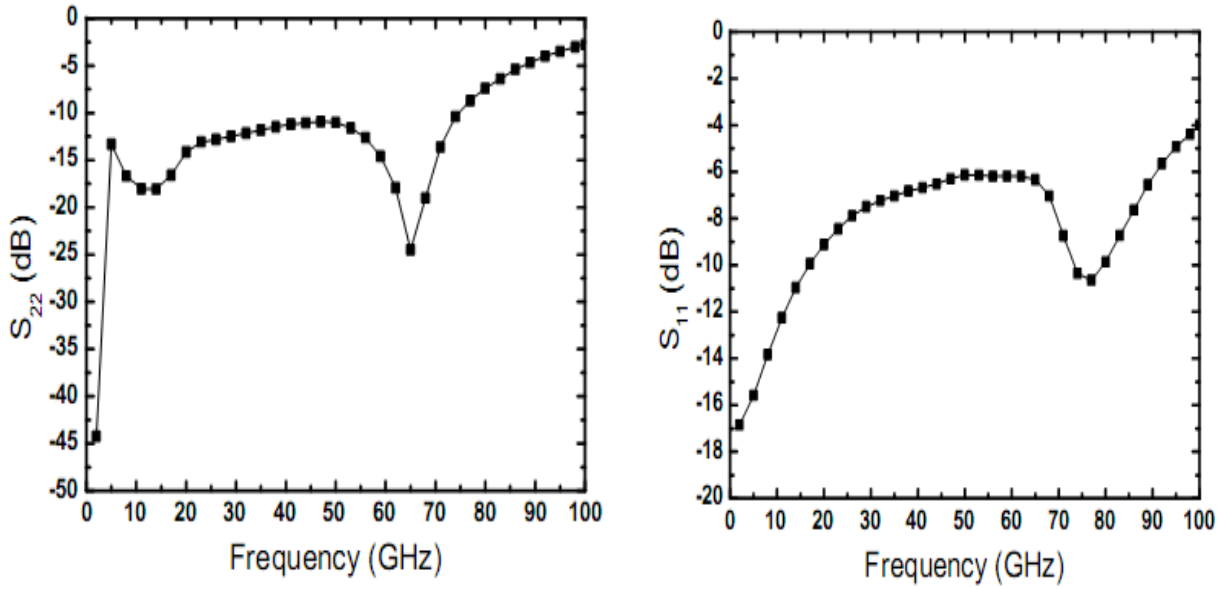

Figure 3.15 *Measured S22 and S11 of the proposed broadband amplifier*

The reverse isolation *S12* is well below -30 dB up to 100 GHz, as shown in figure 3.16.

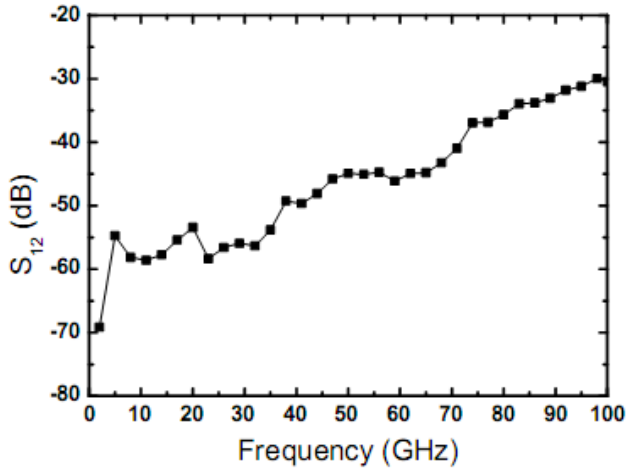

Figure 3.16 *Measured S12 of the proposed broadband amplifier*

Compared to the state-of-the-art CMOS broadband amplifiers, this amplifier achieves the highest gain-bandwidth product (*GBW*) of 231 GHz and the highest GBW/P_{DC} of 2.9 GHz/mW. In addition, the core area is only ~0.05 mm^2, which is also the smallest one compared with other works.

IV. CONCLUSION

Two design techniques are commonly adopted for wideband amplifiers – the distributed amplifier (DA) topology and the inductive peaking technique. The disadvantages of the DA are the relatively large consumption and chip area.

The best bandwidth extension can be achieved by using Asymmetric Transformer peaking. They can simultaneously perform impedance transformation and differential-to-single-ended conversion.

The small die size of 660x380 μm^2 of the 60 GHz Transformer-Coupled Wideband PA, and the chip area of the 70 GHz transformer-Peaking Broadband Amplifier (0.05 mm^2) clearly demonstrates the area benefits of using transformers at mm-wave frequencies.

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