



Topology optimization of planar Integrated Lightwave circuits.

“Optimization through Evolvable Hardware”

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<p>Abstract:</p> <p>The following PhD thesis research has been conducted under the instruction of the Marie Curie Actions research centre at the Numerical Method Laboratory(LMN) program at the "POLITEHNICA" University of Bucharest (PUB), Faculty of Electrical Engineering, Romania. The Electrical Engineering program culminates with the PhD thesis project, which is closely guided by PUB faculty members associated with the Electrical Engineering research centre. This study describes the concept and the result of initial experiments to optimize the topology of a planar lightwave circuit using an Evolutionary Algorithm (evolutionary strategy) with Covariance Matrix Adaptation (CMA-ES), an (search) algorithm for difficult non-linear, non convex optimization problems in a continuous domain. CMA-ES decouples the population size from the problem dimension and hence needs only small populations and relative few fitness function evaluation. The CMA-ES can be described as a randomized black box search algorithm. We use three levels of a sophisticated representation scheme (geometry, functional description and netlist) in combination with scattering approach and driven by an evolutionary algorithm allowing very fast, and accurate simulation of geometrically defined lightwave circuits. Semantic analysis is use to make the transition between the geometry and the functional description by detecting and extracting elements such as, different shapes of directional couplers. Based on this representation scheme a Mixtrinsic Evolvable Hardware (MEHW) method with CMA-ES is proposed, which allows the optimization of the given topology using different operators (mutation, recombination and selection), and with which should be able to search possibilities for evolving into new topologies and solve the portability and scalability problem.</p> <p>The excellent results confirm that the proposed approach concept is an adequate solving method for optimization of planar lightwave circuit structure, whereas the identified weak points of the algorithm indicate possible directions in the future work.</p>	
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STATEMENT OF ORIGINAL AUTHORSHIP

I declared that the work contained in this thesis entitled “The Topology optimization of planar Integrated Lightwave circuits” has not been previously submitted to meet requirements for an award at this or any other higher education institution. To the best of my knowledge and belief, the thesis no material previously publish or written by another person except where due reference is made.

Signed:.....

Date:.....

To my parents:

*“If I take the wings of the dawn,
and settle in the uttermost parts of the sea;
even there your hand will lead me,
and your right hand will hold me.”* Psalms(139:9-10)

Nothing tends so much to the advancement of knowledge as the application of a new instrument. The native intellectual powers of men in different times are not so much the causes of the different success of their labours, as the peculiar nature of the means and artificial resources in their possession¹.

- Sir Humphrey Davy

¹ Quoted from Thomas Hager, force of nature, Simon and Schuster, New York, 1995, p85

SUMMARY

EXPLANATION OF TERMS

LIST OF SYBOLS

Notation	Description

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATION

LIST OF PUBLICATIONS

Chapter 1: Introduction

1.1 Overview

This chapter first presets the motivation behind this research and then details the investigation's specific objectives and the organization of the thesis is detailed.

1.2 INTRODUCTION TO THE AREA AND CONTEXT OF THE RESEARCH

In the design of integrated circuit technology the cost aspect has driven the need of incorporating passive components on-chips and downscaling of the dimensions of the chip. As a consequence of the increased downscaling the industry face a number of challenges in this process [1]. This issue has increased interest in the design process optimization not only in on-chip passive and interconnects patterns. However, also in the optimization of an integrated planar lightwave circuit arise interest. The fabrication cost should be held low while the circuit characteristics have to be met without compromises, the factor of cost is always wanted to be minimized. At the microeconomic level, an increase in design time will increase the productivity results and avoid unnecessary extra mask sets in the developing cycle. The outcomes from improving circuit topology may help to detect or identified design errors in a very timely fashion during the design life-cycle. The design cost can be reduced if the system is able to operate autonomously with minimal or none user interaction, and potentially find solutions that are as cost-effective as optimized integrated planar lightwave circuit and downscaling of the dimensions of the planar lightwave circuit. The topology optimization attempt to integrate geometrical modeling, functional description, netlist and structural analysis into one computer aided design process. This research focus on optimization of lightwave topology circuits based on a sophisticated representation scheme. The levels of representation (geometry, functional description and netlist) in combination with scattering matrix approach and a new method Evolvable Hardware (EHW) may allow a valuable and accurate simulation of geometrically defined circuits. Exploring geometrical elements used to define any filter topology and how to implement EHW in order to optimize the circuit topology.

A semantic analysis makes the transition between the geometry and the functional description by detecting and extracting elements like, e.g., different shapes of directional couplers. Based on this representation scheme EHW will be used for the optimization of a given topology using a number of different mutation operators, and with which should be able to search possibilities for evolving into new topologies.

The topology optimization attempt to integrate geometrical modeling, functional description, netlist and structural analysis into one computer aided design process. This research focus on optimization of lightwave topology circuits based on a sophisticated representation scheme. The levels of representation (geometry, functional description and netlist) in combination with an elaborated Evolutionary Strategy with Covariance Matrix Adaptation (CMA-ES) may allow a valuable and accurate simulation to define any filter topology (Hansen and Ostermeier 1997, 2001). Especially in this context a tool that can take into account the different optimization criteria would be a big advantage (improving quality).

By using self adaptive application (evolution strategies) can help us in selecting the best parameters for to improve the topology. Self-adaptively enables the algorithm to dynamically adapt to the problem characteristics and even to cope with changing environmental as occur in unforeseeable ways in many collaborative development platforms (Thomas Back, 2002) [18]. Evolutionary algorithms consist in population-based global search methods inspired by natural evolution. They are recognized to be enormously efficient for complex non-linear optimization problems. This approach has a promising result for quality assurance and circuit topology optimization of on-chip passive and interconnects patterns. The outcome may have a strong impact on the development cycle.

1.3 APPLICATION OF TOPOLOGY OPTIMIZATION OF LIGHTWAVE CIRCUIT

There are a lot of CAD software for design and helping engineers to simulate and optimize the circuits. Most of this application allocates both passive and optical communications. It reduces the cost in design by creating a physical prototype, to assess design risks, and to assist in the discovery of new products by creating the question “what if” product scenarios. But a real dedicated optimization system is not yet been establish. The optimizer part is based on an evolutionary approach. The particularly combination of forward solver and multi objective optimization give our approach an extra dimension with futures such as building efficient led geometries, intelligent search over multiple parameters optimization. The implementation of forward solver enables an optimizer in combination with the evolutionary algorithm to use information that is available in different abstract level. These make it possible to optimize data on different levels. Because the system can access the information on different levels it is able to transform the topology of the lightwave circuit in order to obtain better and rebust structures.

1.4 PRIOR RESEARCH

Generally, topology circuit design is an iterative process initiated by the perception of geometrical criteria and/or requirements for a physical-based invention, which leads to control and design changes in the development cycle. Design and fabrication should be held low. While the circuit characteristics have to met without compromises, the factor of cost is always wanted to be minimized. At the microeconomic level an increase in design time will increase the productivity results and avoid unnecessary extra mask sets in de developing cycle. The outcomes from improving circuit topology may help to detect or identified design errors in a very timely fashion during the design life-cycle. The design cost can be reduced is the system is able to operate autonomously with minimal or none user interaction, and potentially find solutions that are as cost-effective as possible. Especially in this context a tool that is able to take into account the different optimization criteria would be a big advantage (improving quality). Qualitative validations are often the only ones that can be considered in the hypothesis of very complex environment or materials. In other words, if quality is above satisfaction or expectation, bills are paid on time and firms award this.

There are still some improvements that can be done in design process that meet both qualities standard and budget constraints. It is important to elucidate that evaluating quality for topology design and interconnects patterns need to be validate by the right requirement criteria's that contribute to satisfactory results. For example the benchmarking between high frequency measurements on real structures and high frequency simulations on the respective 3D models is of capital importance for materials, dimension and architecture choice for high frequency applications. The possibility of extending the high frequency simulation to passives with simple interconnect schemes, without going to full-chip modelling is highly desirable for the analysis and the prediction of impedance matching issues both on-chip and on wafer-level packaging [2].

Early studies on Evolutionary Algorithms (EA's) for parameter optimization several optical devices have been optimized with EA's. These are short spot-size converters [3], coupled-cavity semiconductors laser diodes [4], and apodized grating filter [5]. Xie and Steven introduced a method based on evolutionary structural optimization (ESO), and states that topology optimization cannot be misled as easily by poor initial guess. They applied evolution based algorithm for topology optimization [6]. On new interesting method mind in EA's parameter optimization mind be EHW. Past studies on EHW focused on the aspects such as the role they can play in combination of evolutionary computation and hardware design [7], the ability they have [8], and problems they will face in the future. Recent studies such as Higushi and Kajihara pay more attention to seeking valuable applications of EHW, and discover new problems and their corresponding solutions. They illustrate this by combining intelligent computation with some real-world applications of EHW, ranging from analogue to digital chips and from data compression to adaptive control. Further there have been a number of experiments performed on evolving analogue circuits in simulation. To evaluate the circuits a modified version of SPICE simulator was used [9]. The SPICE was able to accurately simulate circuits containing resistors, capacitors, inductors, diodes, transistors,

capacitors, voltage, etc. These applications demonstrate EHW's great potential to provide novel solutions to complex real-world problems.

Elaborating on this, Stoica (1999, 2004) shows a reconfigurable hardware architecture which consist of transistors array, called programmable transistors array. A genetic algorithm was used to specify the connection between transistors. Initial circuit synthesis with Gaussian input-output characteristic [10 and 11]. Koza (1997) argues that it is possible to produce design for quite complex digital and analogue electronic circuits, namely: low-distortion operational amplifier, lowpass, crossover and asymmetric bandpass filters and a cube root circuit.

In his research he use as a starting point typically a simple embryonic electrical circuit containing fixed parts appropriate to the problem and certain wires capable of subsequent modification. An electrical circuit is progressively developed by applying the functions in a circuit-constructing program tree to the modifiable wires of the embryonic circuit (and subsequently the modifiable wires and components of the successor circuits). The functions in the circuit-constructing program trees included (1) connection-modifying functions which changed the topology of the circuit, (2) functions which insert components into the circuit and (3) arithmetic-performing functions which modified the numerical value of components.

The behaviour of each circuit was evaluated using the SPICE simulation program rather than producing a real circuit who's properties were evaluated [12].

1. At the Each connection modifying function in a program tree points to an associated highlighted component and modifies the topology of the developing circuit. Each branch of the program tree is created in accordance with a constrained syntactic structure. Branches are composed from construction-continuing subtrees that continue the developmental process and arithmetic-performing subtrees that determine the numerical value of components. Connection-modifying functions have one or more construction-continuing subtrees, but no arithmetic-performing subtrees. Component-creating functions have one construction-continuing subtree and typically have one arithmetic-performing subtree. This constrained syntactic structure is preserved by using structure-preserving crossover with point typing.
2. Component-creating functions insert a component into the developing circuit and assigns component value(s) to the component. Each component-creating function has a writing head that points to an associated highlighted component in the developing circuit and modifies the highlighted component in a specified way. The construction-continuing subtree of each component creating function points to a successor function or terminal in the circuit-constructing program tree.
3. The arithmetic-performing subtree of a component creating function consists of a composition of arithmetic functions (addition and subtraction) and random constants (in the range -1.000 to $+1.000$) and specifies the numerical value of a component [13].

EHW has only been applied to synthesis of sequential logic circuits. A traditional approach that has been applied for small sequential logic circuits can be subdivided in two main categories intrinsic and extrinsic evolution [14, 15, and 16]. Optimization can be done at different levels. When we talk about optimization we try to look for the answer the question: What need to be done to achieve a desirable outcome or particular target. Previous research has shown that the choice of cell-level analogue circuit topology can have a giant impact on the performance and its implications resonate throughout the rest of the design cycle. A good circuit optimizer can only produce as good as a result as the chosen topology allows [17]. The process of optimization and to choose a topology is an iterative process, and intertwined with choice of specifications. Many combinations may tried for a fixed set of specifications and where areas needed, the specs themselves may be change. One interest aspect is if we could remove the iteration over topology choices by making it part of the search itself but then still the process needs iterations over specs for parameter optimization.

Generally, three types of field solvers are distinguished: the finite-difference-time-domain solver, the finite-integration solver and lattice-gauge solver. The outcome of the field solver is use as a valuable input for determining for determining the parameters of a SPICE network(net list) describing the dynamics of the system under study. Concerning our study we are interested in using evolutionary algorithms to help find

the rules for circuit topology optimization. By using self adaptive application (evolution strategies) can help us in selecting the best parameters for to improve the topology. Self-adaptively enables the algorithm to dynamically adapt to the problem characteristics and even to cope with changing environmental as occur in unforeseeable ways in many collaborative development platforms (Thomas Back, 2002) [18]. Evolutionary algorithms consist in population-based global search methods inspired by natural evolution. They are recognized to by enormously efficient for complex non-linear optimization problems. This approach has a promising result for quality assurance and circuit topology optimization of on-chip passive and interconnects patterns. The outcome may have a strong impact on the development cycle.

Early studies has shown that when implementing the connection scattering matrix method (Monaco and Tiberio 1970) it is possible to combine the whole system into one scattering matrix representing the characteristics of the overall system with respect to the global system inputs and outputs. If implementation of Elementary scattering matrices is used this can be calculated as described in (März 1995)[19].

1.5 CONCLUSION

There has been different type of experiments but still none of them grasp have solve the portability problem from simulations. This is because it is commonly that the experiments based on software are done apart from the hardware experiments. The evolution simulated in software is called off-line EHW here only the elite chromosome is writing to the hardware device (off-chip evolution). On-line EHW the hardware device gets configured for each chromosome for each generation. The genetic operations are done in simulation, while EHW is used to test the fitness of each member of the population. The most commonly methods used for circuit topology optimizations are divided to equation-based and simulation-based methods. EA has shown out of previous experiments to be one of the best candidates used for simulation based optimization. The reason is their adaptability with discrete functions, higher speed comparing with random approaches.

1.6 CONTRIBUTION OF THIS THESIS

The objective of the research is to find out if EHW in combination with solvers can be suitable of circuit topology optimization to reduce the calculation complexity while improving the obtained results. Explore the possibility in multi object optimization true topology optimization.

1.6.1 The academic relevance

The academic relevance for this research is scientifically to help determine the utility of CMA-ES in conceptual design and look whether EHW is suitable for quality assurance in the in topology optimization design. The specific objective is to use EHW drive by CMA-ES to perform structural topology optimization. Evolutionary algorithm may enable us to discover patterns within a specific set of data that allow generalization for self adaptable rules for topology optimization and quality control. It is therefore interesting to see how evolutionary algorithm can be used in the context of circuit topology optimization.

1.6.2 The practical relevance

The practical relevance is the establishment of a better quality assurance process in optimization of planar lightwave circuit topology. Compare the abilities and limitations of this CMA-ES in combination with EHW and forward solver algorithm-based structural optimization approach to those other techniques which have also been devised for automated generation of optimal structure topologies. The result is design faster systems while maintaining the reliability of topologies and anticipate failures in initial design process.

1.7 Problem description

In the process of design and simulations of circuits there is a need to generate a much more “compact” model e.g. a small SPICE circuit, which preserves the behaviour of the passive component, from terminals point of view, for instance the input-output relationship. Design of efficient high speed power circuits is becoming very important. Because the complexity of models in high frequencies quality assurance control has become a crucial process. Currently the EHW is being implemented for general purpose running on different environment (operating systems), but there is not yet a dedicated EHW for simulation of circuit topology optimization. There have been several simulations tools developed such as operational amplifiers, filter, etc, but there is still some gaps in optimization of the result and quality assurance control in the design process.

This research explores the ways that EHW can be implemented to optimize circuit topology and how it can contribute to quality assurance control in circuits topology optimization. Based semantic analysis is will be possible to make transition between the geometry and functional description detecting and extracting elements e.g. like different shape of directional couplers. It's also nice to see how the evolutionary design of representation scheme that allows the optimization of a given topology can only be achieved by integrating results from software simulation (including high quality control) and hardware execution in the same experimental environment (Stoica, 2000). This is why we intent to use EHW in particular the mixtrinsic method. This approach may have the advantage that offering solution that both operate in Hardware and be analyzed in simulations to explore the behaviour outside the domain within which it was evolved originally. This may have a great advantage that the resulting possible new topology is more likely to be portable and test in other environmental platform. The results should give practicing engineers valuable insights into the production on the present simulation.

Topological optimization of integrated lightwave circuits results in a very demanding inverse problem. Besides a smart optimization scheme, a very sophisticated forward solver, which allows the inclusion of a priori knowledge concerning the problem, is mandatory. The solver or optimization algorithms should be able to learn from additional information from the new data. It should get access to the original data, used to trained existence classifiers. It preserves previously acquired knowledge and it should be able to accommodate new classes that may be introducing to new topology. Their exist several implementations of optical filters depending on the specifications there are use in design methods (Oppenheim and Schafer 1989; Jinguji 1996) [17,18]. The three most commonly structures implemented are waveguide grating filters (Dragone 1989) [19], resonant coupler (cascaded Mach-Zehnder) filter (Kuznetsov 1994) [20], and cascaded ring-resonators (Orta et al. 1995) [21]. The problem of all these structures is the large chip space they require. To obtain a desired filter characteristic is easier when using more structural elements or more stages. With a correct topology, however, the required chip space may be reduced.

For every evolvable new topology, the calculation method has to be developed almost from scratch. A system, where the user can just enter the required filter characteristics and then the system would design the most compact filter that meets the given requirements would be very useful. Such a system would solve the inverse problem for the optical filter circuit and has to be composed of a forward solver as well as an optimizer to solve the inverse problem.

In order to build a successful inverse problem solver with mixtrinsic EHW optimization procedure the following conceptual resources are necessary:

- A robust solver that may be able to give useful results for realistic structures;
- A fitness definition which allows a correct qualification of individuals with respect to the given specifications;
- Mutation operators that are able to transform the structures;
- Crossover operators that combine information about several individuals into newly generated ones.

The main idea behind the mixtrinsic EHW is using initially population-based technique from both simulation software and hardware that considers a requirement filter characteristics and output of a schema

as equality constrains that we aim to satisfy. A small sub-population is assigned to each object and layer. After one of these objectives(scheme, etc) is satisfied, its corresponding sub-population is merged with the rest of the individuals in order to minimize that total amount of mismatches produces(between encoded scheme and the truth data) once a feasible individual is found all individuals cooperate its number of gates. The approach mind be very convenient to reduce the amount of computer resources required to design combinational connections of circuits, when compared to others previous research in this area. To obtain a transfer function of a given circuit topology, the geometry need to be first transformed into a functional description, then into a netlist of functional building blocks. Together with the waveguide description, it will be possible to obtain a certain matrix description of the overall filter circuit. Any data that obtained or generated data can be used across different structures can then be introduce into a waveguide database allowing rapid access of subsequentail calculation that are required. The most challenge in this investigation remains in the search of the appropriate schemes or accordingly modifies an element's functionality. Reengineer the circuit while maintaining the connectivity with other operators such as scaling and the predefined functional building blocks.

1.8 DEFINITION OF CIRCUIT TOPOLOGY OPTIMIZATION

The topology optimization of circuit for each candidate design there is associated a structure and a set of parameters for that structure. This topology optimization toward planar lightwave circuit comprises over the entire population of design simultaneously while not requiring that all parameters are requirement or all the structure are fully optimized.

1.9 RESEARCH QUESTIONS

The research is guided by three questions which have been split into two parts. The first is the core question and the two others are sub-questions. The core question which will guide the whole research process is:

Is Evolvable Hardware in combination with solver suitable for circuit topology optimization?

The two sub-questions guiding the investigation are:

1. If the optimization is possible what methods is more appropriate?
2. Is it possible to optimize other parameters e.g filters characteristics and corresponding dispersion at the same time?

1.10 MOTIVATION AND JUSTIFICATION

The motivation for this research is exploring a new methodology that leads to a better filter characteristics and computational efficiency in order to overcome the difficulties of portability problem. The challenge is to implement topology optimization in a cost effective way and a need for more robust solvers that give useful result for realistic structures while being direct compatible with standard IC fabrication techniques. The overall cost of a product is a combination of the design cost and the fabrication costs. Many issues are yet unsolved in the domain of optical devices. Actual optical engineering tools lack of power optimization true increasing of clock frequency and efficiency.

1.11 METHODOLOGY

1.11.1 Implementation and experimentation

Implementation and experimentation with different tools Such as Matlab involving a number of existing simulation methods serves to produce models for netlist.

1.11.2 Literature study

Reading Evolutionary algorithms literature for theoretical considerations on parameters optimization, topology optimization, CMA-ES and EHW trends in evolvable planar lightwave circuits that are extremely useful for valuation as well as for analysis of optimized result.

1.11.3 Interview

Contact with professional circuit developers, researchers, electronic professors, and experts in the field (circuit manufacturers, simulations testers, and chips developer consultancy firms) may be helpful to my research.

1.12 Scope of works

The scope of works includes understanding the theory and concept of Planar lightwave circuits (PLC), the optimization using CMA-ES, EHW advantages and disadvantages and also to justify the measured data.

1.13 OUTLINE OF THE THESIS

The remainder of the thesis is organized as follows:

Chapter 1 provides an introduction to the research. It presents the basic concept, the research objective, methodologies that have been used, and the research approach, which has been implemented in order to evaluate experimental results.

Chapter 2 provides an overview of related work (the necessary background material) on linking EHW to topology optimization of planar lightwave circuit. It introduces the theoretical concept from planar lightwave circuit, and evolvable hardware. This section provides the necessary background material for the understanding the theoretical concept of planar lightwave circuit, optimization. It discusses the processes that are involved in the problem-solving. More precisely, Evolutionary Algorithms are introduced as a general methodology at both fundamental and more advanced level. Various evolutionary techniques are subsequently described from the perspective of how they address the required optimisation aims, and other important issues in Evolvable Hardware are explained, but the overall focus is optimization of structures of planar lightwave circuits.

Chapter 3 provides a study of the state-of-the-art evolvable hardware, CMA-ES and a methodology is proposed to evolve planar lightwave circuit. Covariance matrix adaptation (CMA-ES) is subsequently described from the perspective of how they address the required optimisation aims, and other important issues in CMA-ES are explained, but the overall focus is optimization of structures of planar lightwave circuits.

Chapter 4 provides the experimental result on the case study that is described in Chapter 3.

Chapter 5 the thesis concluded and summarized and suggests a direction for future work.

Chapter 6 provides a list of previous work cited in this thesis.

1.14 RESEARCH APPROACH

A series of activities for a systematic approach has to be performed in order to answer the research question, schematically shown in the research approach below.

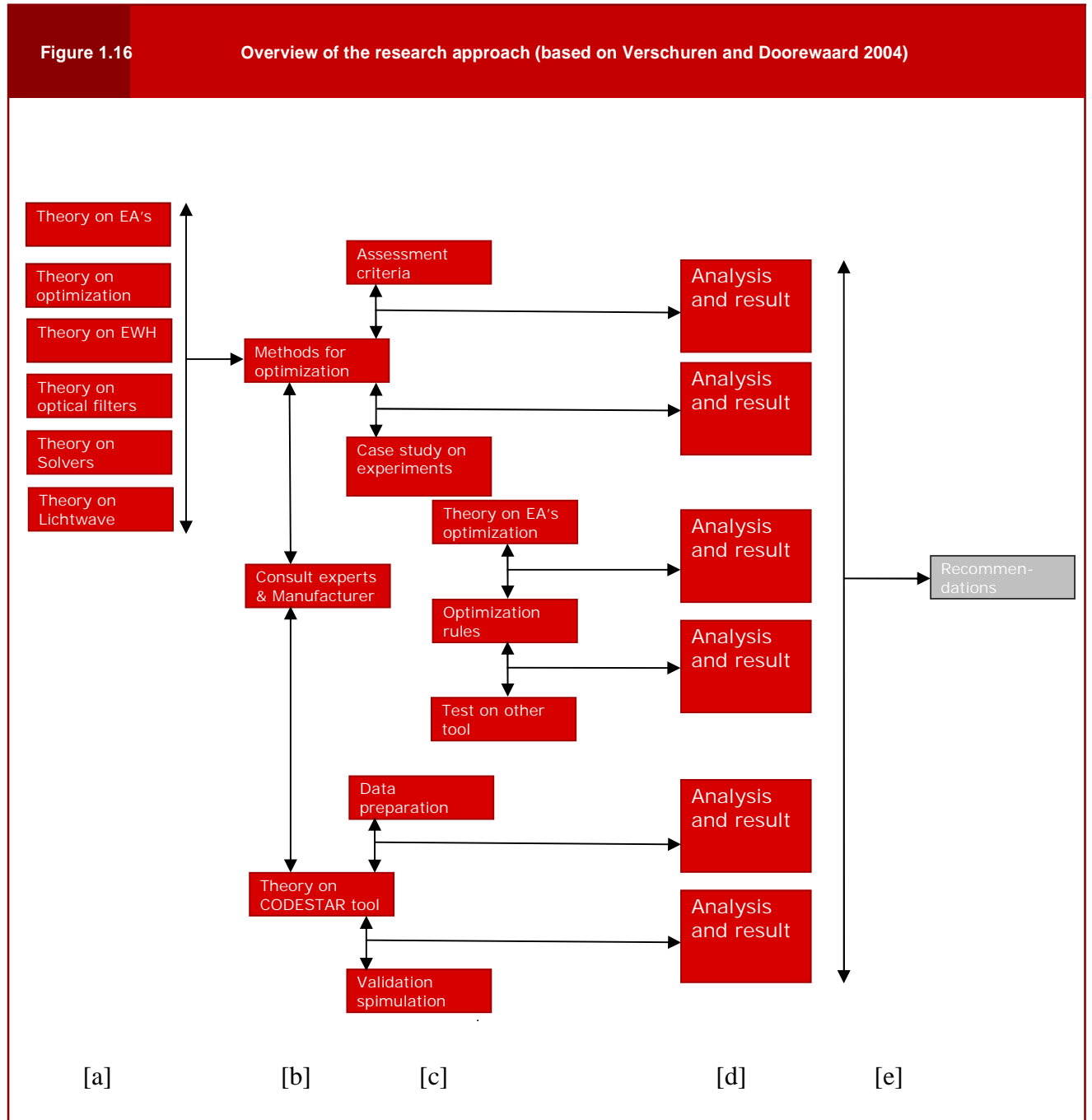


Figure 1.16 overview of the research approach

Part [a]

The first stage of the research is the analysis of several theories for a deeper understanding of the criteria concerning topology optimization, Evolutionary Algorithms, Evolvable Hardware, lightwave circuits, solvers and optimization of parameters. This research leads to answers to the following questions:

Is Evolvable Hardware suitable for optimization of circuit topology? How can we optimize circuit topology (or other parameters of the netlist) while improving reliability and accuracy? How can we lower the cost in the design process?

Part [b]

The second research stage is the analysis of the different techniques of optimization theory (existent condition for optima (minima/maxima), optimization methods (iteratively, step wise or algorithmically) and the study of the Evolvable Hardware process (including the process model Evolutionary algorithm methodology). Experimentation with different development and designing tools. Interviewing and consulting experts in this field is essential to the assessment of the criteria and fault tolerance. The resulting research will answer the following questions:

Which approach of optimization is best at to optimize circuit topology? Which optimization methods are most appropriate?

Part [c]

This is the crucial stage in which the analysis of various, small experiments test, namely a case study of circuit topology optimization. Based on the results of [a] and [b], optimization rules are developed for the use of circuit topology optimization true EHW. This stage will also more clearly illustrate the most efficient methods for evaluating a workable circuit topology. All calculations and data preparation are done during this stage.

Part [d]

Here we will analyse the data gathered on the objects of the research project in order to answer the following questions:

If the optimization is possible what methods is more appropriate?

Is it possible to optimize other parameters e.g filters characteristics and corresponding dispersion at the same time?

Part [e]

In this final stage, conclusions and suggestions will be made based on the findings.

CHAPTER 2: Theoretical background of the research project

This chapter and the next two constitute is the core of the thesis. This chapter give a brief introduction of the basic elements of Evolvable Hardware (EHW), including the pros and pitfalls of implementing evolvable hardware. The following two chapters cover the experimental case study in EHW.

2.1 EVOLVABLE HARDWARE

Evolvable Hardware (EHW) is a new field using an approach in which Evolutionary Algorithm (EA) to search for suitable configuration or design of a reconfigurable device in order to achieve such the circuit behavior which satisfied a particular given specification. It started simultaneously in Switzerland and Japan in the early ninety's and sub- sequential in 1995 in UK. This field was official establish in 1995 and the first international workshop was held in Lausanne, Switzerland. The first international Conference on Evolvable Systems (ICES 96) held in Japan in 1996. EHW refers to hardware that can change its architecture and behavior dynamically and autonomously by interacting with its environment. This concept has attracted increasing attention since it was pioneered by Adrian Thompson at the University of Sussex, England in the early 1990's. Thomson toned a reconfigurable hardware (a Boolean logic device) using fewer than 40 programmable logic gates and no clock signal in a field programmable gate arrays (FPGA's). Thomson also highlighted the importance that temperature plays, as it can affect the responses of the circuit elements. EHW has been shown to be able to perform a wide range of a task from pattern recognition to adaptive control. Zebulum shows with his research different platforms (e.g. general propose versus dedicated programmable hardware) and different methods (e.g. GA's, GP's and Evolutionary Programming) [2]. A set of problems are discussed that could be used to assess an evolvable system's potential against other systems. This field of EHW has emerged from a range of other fields. The most important are shown in fig.1. There is much interchange of concept between the fields of evolvable hardware and bio-inspired hardware, but EHW lies at the crossroads between all three of this major science.

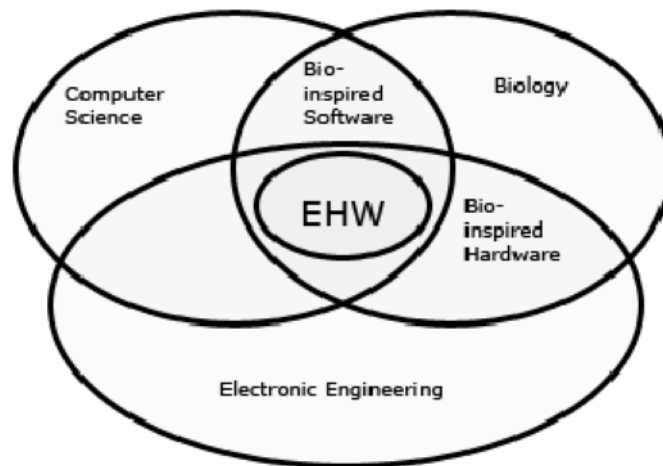


Fig.1: The field of evolvable hardware originated from the intersection of three sciences

The three major aspects to EHW are simulated evolution and electronic hardware. We can classify this into extrinsic, intrinsic and mixtrinsic EHW. Extrinsic EHW simulates evolution by software and only downloads the best configuration to hardware in each generation (i.e., the hardware is only reconfigured

once). The Extrinsic EHW proposed by Kalganvoa a Miller is used to generate the combinational part of a sequential logic circuit [x]. The ultimate goal is to simulate all the circuit to see how they perform (evaluating their fitness function of the resulting circuit). Intrinsic EHW simulates evolution directly in its hardware. Physical tests are run on the actual hardware (i.e., every chromosome will be used to reconfigure the hardware. The EHW will be reconfigured the same number of times as the population size in each generation). Mixtrinsic EHW is a method of modeling, which allows simultaneous development of coherent models (combination technique that combines the intrinsic and extrinsic modes). This method use a mixed population of both software models and reconfigurable hardware ware(candidate solutions may have different levels of resolution or perhaps even of very different in nature). One approach is to assign the solutions to alternative instantiations of different resolution changing from a generation to another. Another approach is to have a combined fitness function that characterizes the modeling ensemble (i.e. each candidate solution in all its instantiations at different levels of resolution). The simulated evolution is most of the time driven by EA(evolutionary programming, genetic algorithms, evolutionary programming or evolution strategies), using algorithms that are inspired by biological evolution. There is no uniform answer as to which one of the EA would be the best for EHW. This new approach can help preserve existing functionality in changing operational environment to compensate fault, aging or perhaps temperature drift and high-energy radiation damage. Once a clear example were EHW can directly provide benefits is deep down in the ocean or in the space were in particular the environmental condition can change dramatically (e.g deep space probes may encounter high radiation environments, which can alter circuit performance and this can have a catastrophic impact on spacecraft). Most EHW relies heavily on reconfigurable hardware, such as FPGA's. The architecture and functionality of an FPGA are determined directly by its architecture bits. These bits are reconfigurable. EHW makes use of this flexibility and employs an evolutionary algorithm to evolve these bits in order to perform certain tasks effectively and efficiently.

2.1.1 The mixtrinsic multi-Objective evolution

As we in paragraph 2.1.1 described the extrinsic evolution cannot cope with all the system deviations, while evolving the system intrinsically requires measuring the hardware specifications with measurement assessment circuits (in our case the topology structure). Measuring some of the hardware specifications requires most of the time expensive equipment and is also a time-consuming approach.

Thus, a novel approach is proposed that divides the hardware specifications into two sets [TK07].

This set of specifications is evaluated extrinsically. If the target specifications over fulfill the application requirement, the influence of deviations on this set of specifications does not lead to any dramatic specification variation.

The second set of specifications contains the specifications that are sensitive to deviations and can cause direct distortion in the signal, while they are easy to measure at low cost such as offset, swing output voltage, common mode range (CMR), etc., For example, the change of the CMR due to deviations can cause signal distortion, and the offset is very sensitive to deviations and cannot be handled with simulation. This set of specifications is measured intrinsically. The optimization criteria are multi-objective optimization where each individual has intrinsic and extrinsic objectives as shown in figure 5.6. (a)

Classification in Evolvable Hardware

	EHW	Intrinsic	Extrinsic	Mixtrinsic	Complete
EA					
Chromosome representaiion		Hardware	Software	Hardware Software	Hardware
Evolutionary Algorithm		Software	Software	Software	Hardware
Evaluation		Hardware	Software	Hardware Software	Hardware

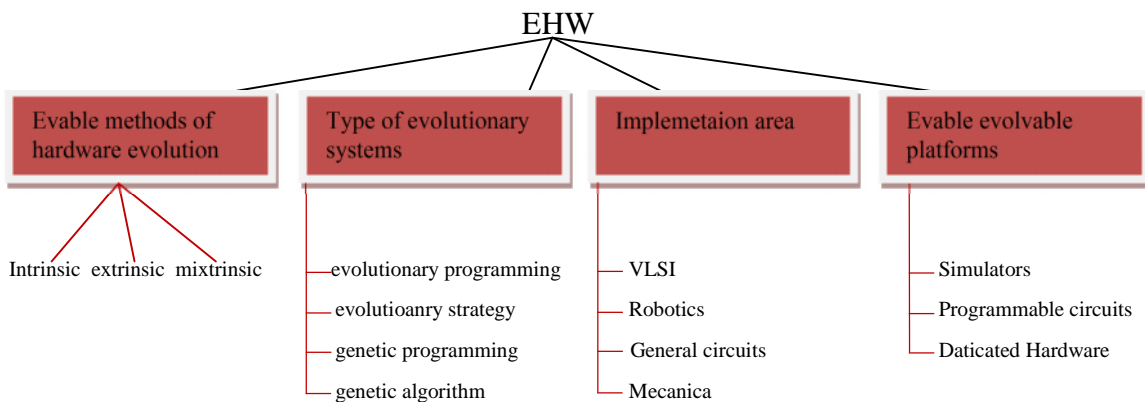
Table 2.1.1

2.1.2 Abstraction level

What does an EHW system evolve? EHW utilizes Evolutionary Computation (EC) technique to autonomously evolve hardware circuit structure that can be applied to solve real-world circuit design experiments. There are two main categories for abstraction level of EHW evolution.

First is the chromosome encoding in the evolutionary algorithm. This can be either direct or indirect representation of a circuit. The evolution in indirect representation of the circuit can reduce the size of the search space significantly. Indirect representation of a circuit will always introduce constraints that can be evolved. Secondly, the use of primitives in the circuits. When a low level of primitives are used the possibility to evolve very efficient circuits. However, if the primitives are too low level, the change that a circuit can be evolved is very small. Driven by an Evolutionary Algorithm (genetic algorithm, evolutionary program, evolutionary strategy, etc.) an EHW system evolves circuit structures by providing digital blueprints (chromosomes) that are recreated and altered at every generation by genetic operators. The Field Programmable Gate Array (FPGA) architecture allows dynamic reconfiguration of low-level digital resources and remains an ideal platform for EHW simulations.

2.1.3 Evolvable Hardware Taxonomy



2.2 Hardware description language (HDL)

The HDL syntax is a programme language for description of electronic circuits. HDL includes explicit notations for expressing time and concurrency, which are the primary attributes of hardware. Further it contains characteristic that allow expression of circuit connectivity between hierarchies of blocks which can be properly classified as netlist languages used on electric computer-aided design (CAD). HDL is used to write executable specifications of some piece of hardware. An Evolutionary Algorithm can evolve a HDL-program in the form of Abstract Syntax Trees (AST). The crossover in such an algorithm is very restricted by the grammar of the language. The crossover point in both parents has to select sub trees so that offspring's are created with a correct syntax (e.g. Hemmi et, al. 1994 and 1996).

HDL-simulation enabled engineers to work at a higher level of abstraction than simulation at the schematic-level, and thus increased design capacity from hundreds of transistors to thousands[x and y].

2.3 The strengths of using EHW in topology optimization of planar lightwave circuit.

EHW approach offers a number of advantages over traditional circuit design ones used although the aim might be to develop a EHW that adapts in a real physical environment and simultaneously learns from his new data. This characteristic behaviour offers exploration in a much wider range of design alternatives than those considered used by conventional design methods (by a human being, formula's, etc.). This has been shown in different experiment in other design tasks, such as design of neural networks [4, 5, 6, 7, 8], or of building architectures [9].

The first advantage is that the EHW design approach does not assume *a priori* knowledge of any particular design domain. It can be applied by users without resorting to domain experts. It can be used in domains where little *a priori* knowledge is available or where such knowledge is very costly to obtain.

Secondly, the EHW design approach is very flexible. Because it can deal with non-differential or even discontinuous objective functions. It can deal with various linear and nonlinear constraints as well as objectives. Its population-based nature makes it ideal in tackling multi-objective design problems.

Although the evolutionary approach can work with little *a priori* domain knowledge, it can incorporate domain knowledge in the chromosome representation and search operators easily if such knowledge is available.

Third, the EHW approach can offer a radically new design (unreachable by conventional techniques) can be discovered by the means of EA.

Fourth, "The challenge of conventional design is replaced with that of designing an evolutionary process that automatically performs the design in our place. *This may be harder than doing the design directly*, but makes autonomy possible." (A. Stoica) EHW can be reconfigure its structure dynamically (on-line) and autonomously, according to changes in the task requirement or the environment in which the EHW is embedded [8]

2.4 The pitfalls of using EHW for circuit topology optimization.

All components may eventually fail at a certain point. Some failures cause no perceptible effect on a chip behavior, whereas in other cases failures or the wrong choice can produce very obvious changes from mild to total destruction in circuit design. When devices sizes shrink and lines in design come closer together causing sometimes increasing the chance of undesired cross talk between two metal lines(that connect different transistors). The increased clock frequency induces a stronger electromagnetic coupling between different parts of design. The substrate can act as a transparent medium for electromagnetic waves, thereby causing undesired exchange of energies between runner in design. The reliability and availability in the design process are trying to make a fault tolerant (FT) avoiding this scenario. Considering this into account we define a circuit design is FT if it can continue to operate in the presence of failures (perhaps degraded performance).

Another challenge is EHW's scalability concern with computational complexity of an EA. Currently in some experiments it is not unusual to carry out an EHW experiment that runs for days. Yet the EHW used in these experiments contained only 100 functional components, topologies or so. The question is: how long will it take to evolve an EHW with 10 000 circuit topology to find an optimum point (this count also for functional components) using the current techniques?

Sometimes a fitness function that guarantees the circuit topology correctness is very difficult to find without incurring a heavy computational costs in fitness evaluation.

Early experiments have shown that the solution obtained by evolutionary design may suffer from a portability problem. For example, it was observed that some circuits or topology through evolutionary design on a Hardware(HW) platform had different behavior when they are tested on a second platform, although the two were of similar type/construction . This means that the circuit topology evolved did not reproduce the same behavior when tested on another platform. In many of the circuit topologies resulting from intrinsic evolution do not produce a good response (as obtained in the real HW) when they are simulated in SW.

One reason behind the portability problem is that, in each case, evolution finds the easy way out, optimizing for whichever raw material is given. The portability problem between two HW platforms is

strongly related to differences in a set of characteristics that evolution exploited in one platform and cannot exploit a different one.

2.5 Evolving in simulation

The EHW can be best expressed as a black-box view of a problem. The idea from this point of view is that regarding the black box it should be such that on presentation of the original input signals and the desired outputs are delivered. The details inside the black box are encoded into chromosomes. The evolution of electronic circuits is based on a population of competing designs, the best ones (i.e. the ones that come closer to meet the design specifications) being selected for further investigation. Each candidate circuit design is associated with a "genetic code" or chromosome. The simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. The first step of evolutionary synthesis is to generate a random population of chromosomes.

The chromosomes are then converted into a model that gets simulated (e.g. by a circuit simulator such as SPICE) and produces responses that are compared against specifications. Or, the chromosomes are transformed into a configuration bitstring downloaded into a programmable device.

The configuration bitstring determines the functionality of the cells of the programmable device and the interconnection pattern between cells. Circuit responses are compared against specifications of a target response and individuals are ranked based on how close they come to satisfy it.

We can devise two methods to represent circuits using SPICE netlists: using models of programmable devices or using an unstructured representation. In the former, a binary representation is employed to provide the state of the switches of the configurable device.

The unstructured representation establishes a straightforward mapping between the electronic circuit topology and the integer strings processed by the ES. Each functional block of the string, also called gene, states the nature, value, and connecting points of a correspondent electronic component, which may include resistors, capacitors, bipolar transistors and MOS (Metal-Oxide-Semiconductor) transistors.

2.6 Evolving platform

2.7 ANALYSIS AND OPTIMIZATION OF PLANAR LIGHTWAVE CIRCUITS

Planar lightwave circuits (PLCs) are optical devices that control and route light-signals along prescribed pathways through a microchip. PLCs are ideally suited for optical signal generation and processing, which employ optical waveguides to confine and steer light through on-chip processing elements such as power splitters, interferometers, switches, and modulators [m,n]. Because of the ability to amalgamate these components onto a single substrate, PLC technology is also called integrated optics. The microsphere resonators, primarily demonstrated so far coupled to tapered fibres, have the potential to become key components in photonic circuits, providing feedback, wavelength selectivity and energy storage to allow dispersion control and enhanced nonlinearity, resonant filtering, waveguiding with low bend radius and ultra-low threshold lasing. Many of these properties stem from strengthening the interaction of light with the material through high-Q resonance. Planar lightwave circuits present an ideal platform for the precise placement of individual microspheres or arrays of microspheres, to realise highly functional circuits in a more robust configuration than fibre devices.

2.8 THE FORWARD SOLVER CONCEPT

As illustrated in Fig 2.3.1 the forward solver need to relies on the top of serveral design representaion schemes. There are model four representaion schemes : (1)The geometry description, (2) the functional description(semantic description), and (3) the netlist [25].

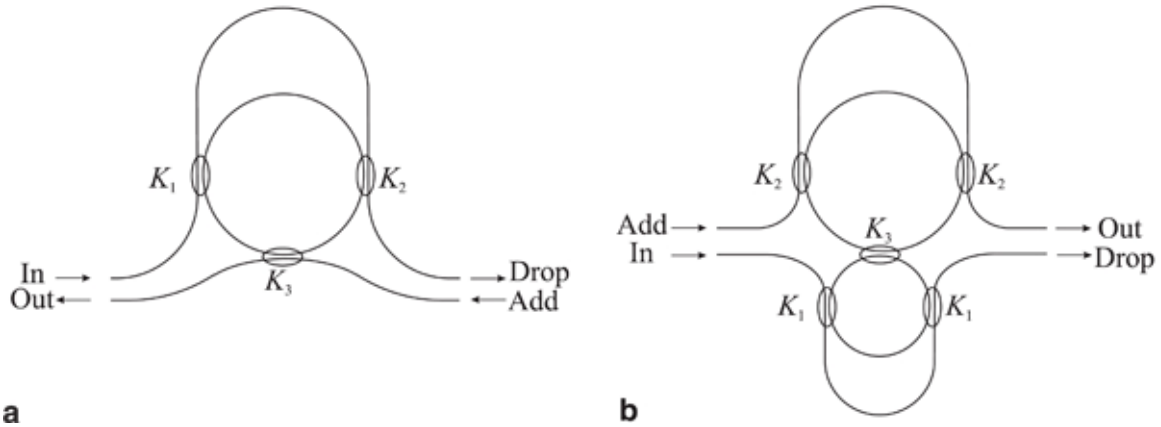


Fig. 2.3.1 shows two examples of filters composed of ring resonators which are more compact than standard design using waveguides and directional couplers. The couplers are encircled. (a) Triple-coupler ringbased waveguide resonator (Barbarossa et al. 1995a), (b) compound triple-coupler ring resonator (Barbarossa et al. 1995b) [25].

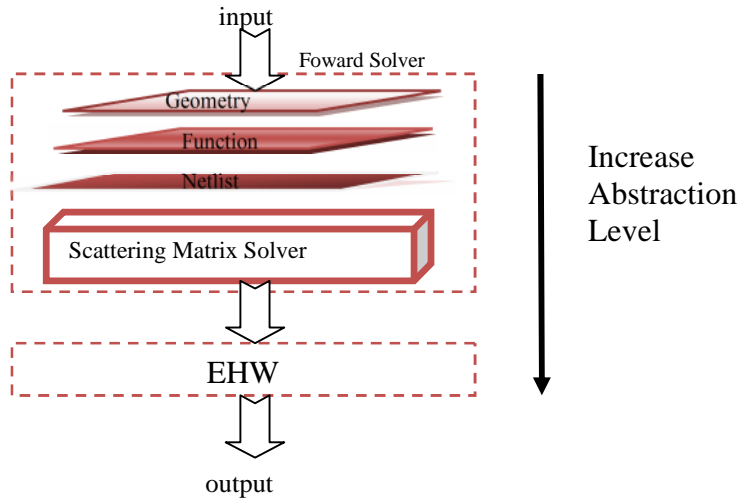


Fig. 2.3.2 the architecture of forward solver including the four levels of representaion. They can be seen as different level of abstract of the same structure containing more (like a container) and more information about its functionality

The three representation levels into the foward solver enables to act on the geometrical structures and make possible the transition between the three abstraction levels there are two functions: (1) the sematic analyser and (2) the netlist generator. The implemetaion of the components will be descuss later on in this paper on paragraph 2.4. In order to optain the transfer function of a given circuit topology, the geometry is first transformed into a functional description, after this into a netlist of functional building blocks. In combination with the waveguide description, it is now possible to obtain a scattering matrix description of the overall filter topology. This data information is use as the initialization of our population. Further any data can be used across different structures which introduced in the into a waveguide database (WDB) to allow rapid access for subsequention mutations such as information includes effective indices, eigen modes and coupling coefficient. See fig. 2.2.3 for the flow diagram.

2.9 THE INGREDIENTS FOR OPTIMIZATION USING EHW

According to Fig 2.2.2 en 2.2.3 we will proceed in this paragraf to explain the different representaiton levels, starting with the geometric description of the waveguide circuit, contiuiing with the sematic analysis, then the scatering matrix approach and how this is pass end combine with EHW.

2.9.1 The wave guide description

In the wave guide description, a standard attribute with has to be defined. To obtain others widths, all brinks are modified. From the waveguide description the eigenmodes and the effective indices are computed using the imaginary-distance beam propagation method[x], whereas the coupled- mode theory allows coupling coefficient of directional couplers to be determined. These values are used to calculate the scattering matrix elements of various functional structures[y].

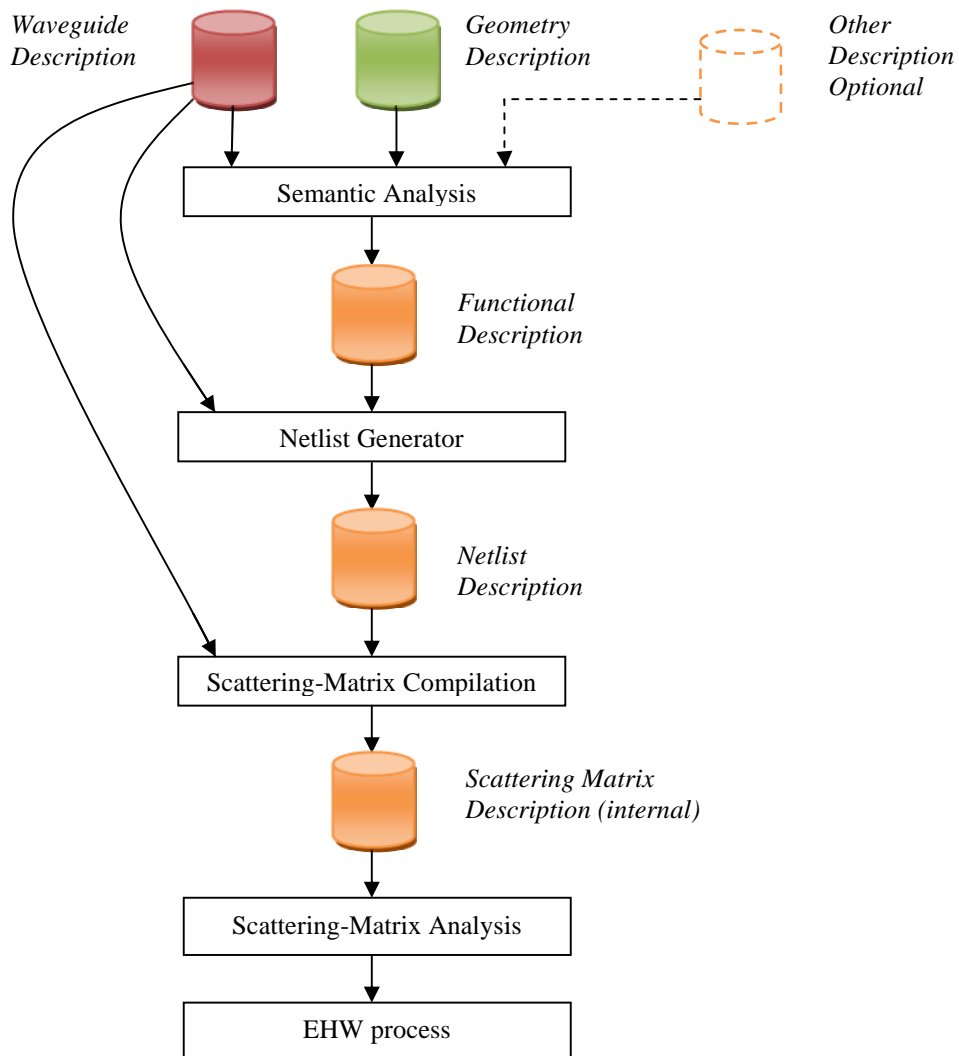


Fig. 2.4.1 shows the flow for forward solver including the EHW. For further detail of the EHW process look to fig. 2.4.5.1

For the circuit topology optimization forward solver mind be not enough because a the follwing issues: a forward solve $p = g(x(p), p)$ can only give point wise information, it can't tell you what you ultimately want to know in the topology circuit optimization. Question such as:

- How to characterize the error in the original model so that it can be improved? Error estimation

- What is the uncertainty in x or p $g(x(p), p)$ given uncertainty in p ? UQ
- What is the best value of p so that my model $f(x, p) = 0$ fits exp. Data? parameter estimation
- What is the best value for p to achieve some goal in any layer? Optimization

2.9.2 The geometry description

Generally the most of the filter topology can be represent as concatenation three generic elements which are straight, bent and tape. The last one is introduce to adapt for different waveguide widths. This means that combining this 3 waveguides you can construct virtually any planer lightwave circuit. To keep it simple its important that only the basic description is used(very simple building blocks). In the geometry defination, absolute coordinates are given for all the elements. One of the constrains is that at this point no connectivity check is done. This will be out of the scope and is the responsibility of the system user to define geometry structures that are correcty convertible into functional description.

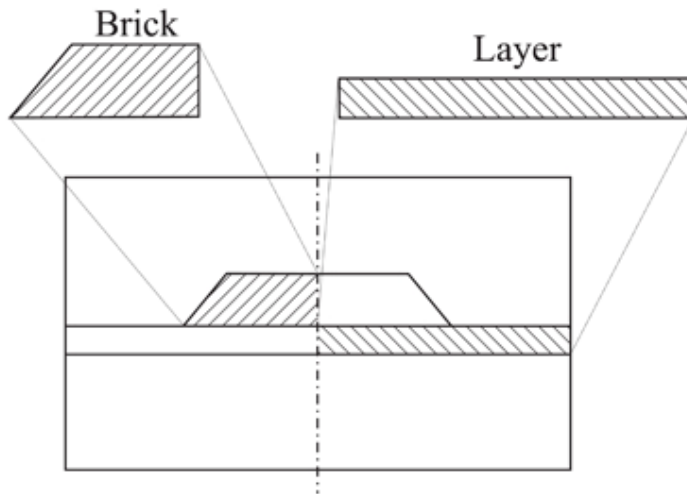


Fig.2.4.2.1 Example of a waveguide structure composed of layers and bricks. Source is been extracted of early experiments [25].

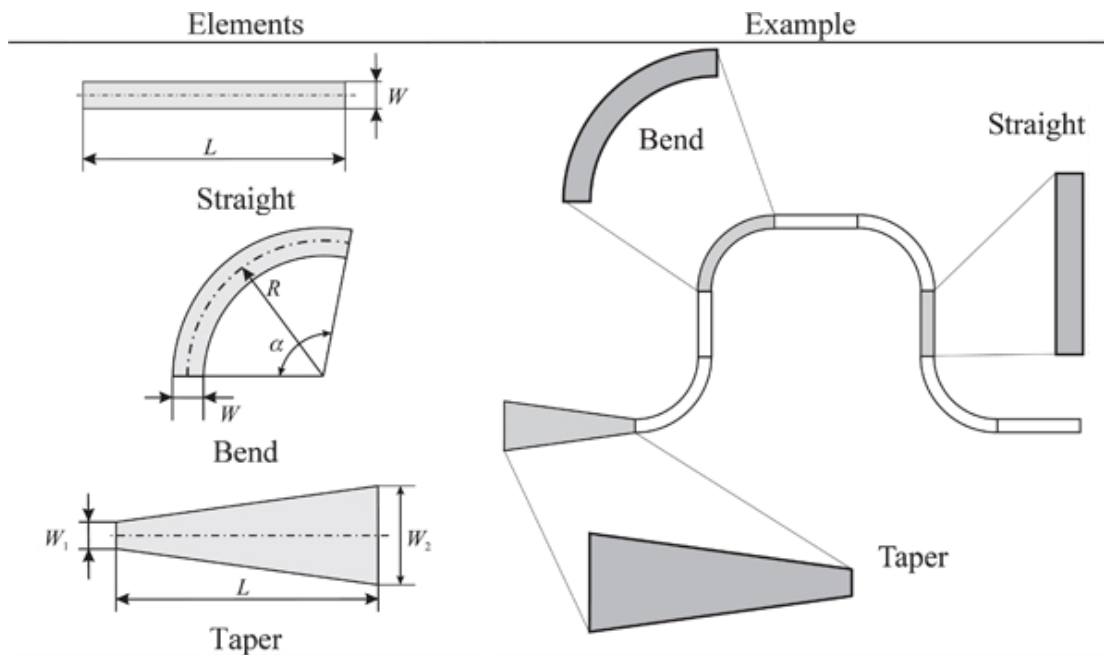


Fig.2.4.2.2 defination of the geometry elements used to define any filter topology as well as an example of a circuit composed of these elements [25].

Defination of the geometry elements to define any filter topology. The geometry contain information about the start point and end point of the element. The general variables used are (X_1, Y_1, X_2, Y_2, W) define the start and end point of the element.

Elements	Description
Straight	X_1, Y_1, X_2, Y_2, W
Bend	X_1, Y_1, X_2, Y_2, W, R (if $R = 0$ then the sign of defines the bending direction)
Taper	$X_1, Y_1, X_2, Y_2, W_1, W_2$

Table 2.4.1.1

2.9.3 The sematic analyzer and the netlist

The challenge in optimization relies in allowing a program to find the function of any possible topology. This hard task could be performed by a user in were they easily distinguishing can be done between different elements like couplers a Y-branches by simple observation of the picture. The geometric description does not contain any data information about functionality of the structure. The task of the semantic analyzer is to scan the geometry for different functional relations between waveguides and decorates the abstract syntax by attaching attribute's values (e.g. various couplers or nodes). It is required to define a set of functional elements with which any planer lightwave circuit can be constructed (see fig. 2.3.3.1. different functional element is given). Constraints are associated with each functional element to define the limits of applicability. These constrains are stored in a wave guide library which is linked to a waveguide definition. The corresponding values can be defined according to measurements or experience. At the functional description level all geometric information which allows the placement of the elements are described, and it contains also the functional information about coupled elements (see parameters in see fig. 2.4.3.1). The geometry elements are cut accordingly to obtain the functional elements. In generally every filter construction can be design out of directional couplers and connecting waveguides. Ones the sematic analyzer has created the functional description next step is the generation of a netlist. It defines the connectivity between the functional elements. The netlist definition contains a minimal set of parameters necessary to completely describe each element. Additionally the input and output ports are numbered to define how the elements are connected. The netlist generator automatically detects any global input and output ports. The program can then transform the netlist description back into a functional description and into geometry. This will be necessary for the operation of EHW. It must be guaranteed that the transformation back and forth does not modify the geometry of the structure. If any illegal constellation of geometric elements is detected by the semantic analyzer, an internal error code is generated. Thus the EHW can eliminate illegal structures [25].

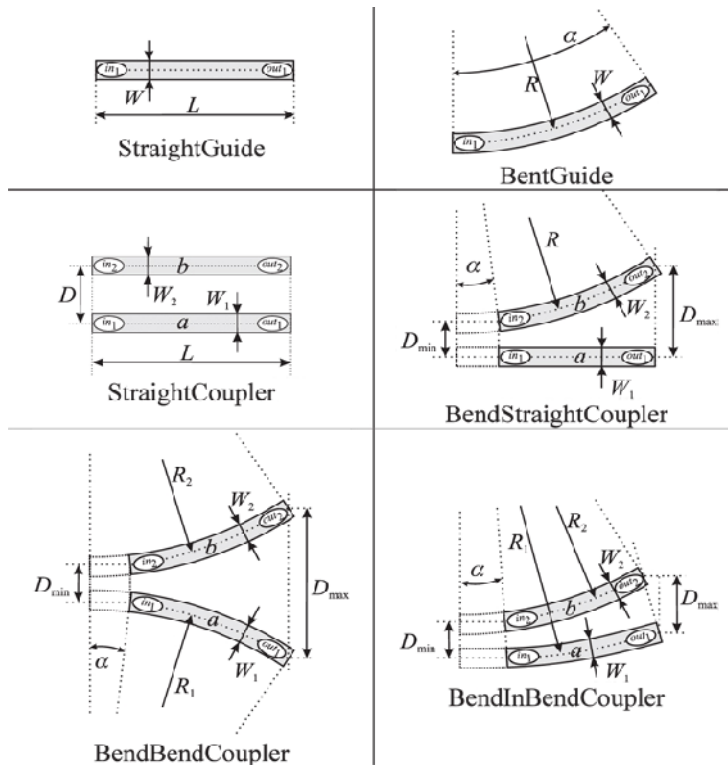


Fig. 2.4.3.1 Simple of functional elements used by the semantic analyzer to extract the function of any filter topology. in_x and out_x are the interface nodes of the elements.

Definition of functional elements used by a semantic analyzer in order to extract the function of any filter topology. The general variables are X_1, Y_1, X_2, Y_2 define the start and the end point of an element in_1 and out_1 represent the interface nodes of the functional elements used

Elements	Description
Straight	StraightGuide (in_i) - \rightarrow (out_i) (L, W) StraightGuide X_1, Y_1, X_2, Y_2, W
Bend	BendGuide (in_1) - \rightarrow (out_1) (R, α, W) BendGuide $X_1, Y_1, X_2, Y_2, W, R, \alpha$
Coupler	StraightCoupler (in_1, in_2) - \rightarrow (out_1, out_2) (D, L, W_1, W_2) StraightCoupler ($X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, W_1, X_{1b}, Y_{1b}, X_{2b}, Y_{2b}, W_2$)
BendCoupler	BendStraightCoupler (in_1, in_2) - \rightarrow (out_1, out_2) ($L, R, D_{min}, D_{max}, W_1, W_2, \alpha$) BendStraightCoupler ($L, X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, W_1, X_{1b}, Y_{1b}, X_{2b}, Y_{2b}, R, W_2$)
BendCoupler	BendStraightCoupler (in_1, in_2) - \rightarrow (out_1, out_2) ($2, R, D_{min}, D_{max}, W_1, W_2, \alpha$) BendStraightCoupler ($2, X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, W_1, X_{2b}, Y_{2b}, W_2$)
BendBend	BendBendCoupler (in_1, in_2) - \rightarrow (out_1, out_2) ($R_1, R_2, D_{min}, D_{max}, W_1, W_2, \alpha$) BendBendCoupler ($X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, R_1, W_1, X_{1b}, Y_{1b}, R_2, W_2$)
BendInBend	BendInBendCoupler (in_1, in_2) - \rightarrow (out_1, out_2) ($1, R_1, R_2, D_{min}, D_{max}, W_1, W_2, \alpha$) BendInBendCoupler ($1, X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, R_1, W_1, X_{1b}, Y_{1b}, X_{2b}, Y_{2b}, R_2, W_2$)
BendInBend	BendInBendCoupler (in_1, in_2) - \rightarrow (out_1, out_2) ($2, R_1, R_2, D_{min}, D_{max}, W_1, W_2, \alpha$) BendInBendCoupler ($2, X_{1a}, Y_{1a}, X_{2a}, Y_{2a}, R_1, W_1, X_{2b}, Y_{2b}, R_2, W_2$)

Scattering Matrix Analysis

The main concept of Scattering is taken from the game billiards(also called pool). One takes a cue ball and fires it up the table at a collection of the other balls. Right after the impact, the energy and momentum of the cue ball is divided between all the balls involved in the impact, The cue ball scatters the stationary target balls and in turn is deflected or scattered by them. In a planar lightwave circuit topology optimization, the equivalent to the energy and momentum of the cue ball is the amplitude and phase of the incoming lightwave on a transmission line. This incoming lightwave is scattered by the circuit and its energy is partitioned between all the possible outgoing lightwave on all the other transmission lines connected internal and external nodes of the circuit. The scattering parameters are fixed properties (individual blocks) of the circuit which describe how the energy couples between each pair of external and internal nodes or different elements connected to a circuit. The netlist represents a number of individual building blocks connected to each other by ideal links. Each of them can be represented by an individual scattering matrix. Assuming that the whole system is single mode, only one port is required for each interface node. Fig. 2.4.4.1 shows a structure of such connected scattering matrices.

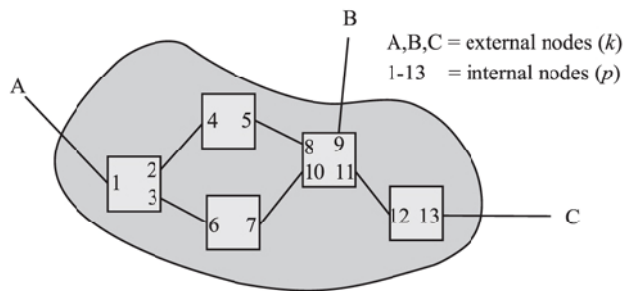


Fig. 2.4.4.1 Lightwave circuits are composed of several elements. These can be combined such that an overall scattering matrix can be defined representing the relationship between the external ports.

Using the connection scattering matrix method (Monaco and Tiberio 1970) it is possible to combine the whole system into one scattering matrix representing the characteristics of the overall system with respect to the global system inputs and outputs. Elementary scattering matrices are calculated as described in (März 1995). Since the individual scattering parameters are wavelength dependent, it is more efficient to evaluate the expression analytically before sweeping over the wavelength. Any calculated value that does not change for one wavelength is cached. Therefore for one wavelength different scattering matrix parameters can be calculated with negligible computational effort.

$$[X]_{\text{tot}} = \begin{bmatrix} [X]_1 & [0] & [0] & [0] \\ [0] & [X]_2 & [0] & [0] \\ [0] & [0] & [X]_3 & \cdots [0] \\ \vdots & & & \ddots \\ [0] & [0] & [0] & [X]_n \end{bmatrix}$$

$[X]_i$ is the scattering matrix of many elements (i) and n is the total number of elements the rows and columns of $[X]_{\text{tot}}$ are then rearrange to place the external nodes in the uppermost lines and in the leftmost columns. With operation $[X]_{\text{tot}}$ is divided into four parts $[X]_{kk}$, $[X]_{pp}$, $[X]_{pk}$, and $[X]_{kp}$

In a_i and b_i represent the incoming and outgoing waves respectively of the port i . $[X]_{kk}$ depends on the external ports only and $[X]_{pp}$ depends on internal ports only. The other two ($[X]_{pk}$ and $[X]_{kp}$) refer to external and internal ports.

$$\begin{bmatrix} b_1 \\ \vdots \\ b_k \\ \vdots \\ b_n \\ b_{n+1} \\ \vdots \\ b_p \\ \vdots \\ b_z \end{bmatrix} = \begin{bmatrix} [X]_{kk} \\ [X]_{pk} \end{bmatrix} \begin{bmatrix} a_1 \\ \vdots \\ a_k \\ \vdots \\ a_n \\ a_{n+1} \\ \vdots \\ a_p \\ \vdots \\ a_z \end{bmatrix}$$

To make the connections between the internal ports a connection $[C]$ is needed. The matrix $[C]$ the same dimensions as $[X]_{pp}$. The value 1 is inserted wherever two port are connected.

2.9.4 The WaveGuide Library and Waveguide Database

The waveguide library include information about the constrains (e.g minimum and maximum waveguide widths minimum radius for bend and other condition for detection of couplers). In order to accelerate the calculation a database containing data such as coupling coefficient information can be used. The solver or the evolutionary algorithms can access this data without the need to recalculate certain measurements needed. When certain data is missed the corresponding solver can be applied and this can be introduced into the database. With this approach the forward solver can continue its calculation without any problem.

2.9.5 The calculation of the Coupling Coefficient

2.9.6 Elementary Scattering Matrices

2.9.7 The EHW process

This section introduces the concept of implementing EHW in the process of optimization. It is provided only as a guide and is not intended as a substitute for any other approach for topology optimization.

In the execution of the EHW we can categorize this process in two stages: the preparation stage and the search stages. In the preparation stage a set of population must be prepared because the evolutionary algorithm uses parallel search methods that start searching from their initial candidate population. The population will be initialized with random values, possibly seeded with some known good solutions that perform well from previous simulation tests. The initialization of the population for EHW by using a mixture of models will use a heterogeneous mix of models of various types e.g. of both upper and lower limits. This is done by using models composed partly by simulation and hardware. This helps a better fitness in the simulation process producing a desired behavior outside the domain that is being developed. Each individual in the population is often called a chromosome or genotype. We can look at this as the DNA of the data is represented by an array of bits. Each bit in the array is often called a gene. The success of the optimization problem depends on the representation, diverse operation such as the chromosomes, fitness function, method of crossover, mutation operation and different information from the chromosome. While the mutation adds new information to a chromosome, it also destroys useful information held in the chromosome with the illusion to create better generations (offspring).

2.9.7.1 Chromosomes

Thus, the chromosomes contains all the information nesecary to descripbe an individual which in our case is a representation of a circuit with a set of components, different layer description and their interconnections. The chromosomes are composes of genes as we mation before for the various characteristics to be optimized and can be any length depending on the number of parameters to be optimized.

2.9.7.2 Encoding

Encoding defines the way each gene is stored in the chromosome containing the functional description of a given circuit and translated to actual problem parameter. The description is build by using a fixed-length that specified a number of logic elements presented to the framework. From this the desired circuit topology functionality must be generated. A possible encoding schem for a hypothetical circuit topology using a 16 bit binary chromosome is shown in the illustration below:

11101	11	000 110	101
Gene for bias xyz	Gene for xyz	Gene for xyz	Gene for capacitance

Fig. 1.4.5.2 Encoding Example

2.9.7.3 THE FINTNESS DEFINATION

An evaluation function, known as the fitness is used to evaluate each chromosome in terms being a single numerical quantity describing how well an individual meets predefined design objectives and constraints (being a good solution to the related problem). Fitness can be computed based on the outputs of multiple analyses using a weighted sum.

The defination of the desired filter charatereistics is a linear function in the linear scale(see fig xyz). Each part of the defination consists of either an upper or lower limit and weight factor that defines the importance of the limit. Each scattering parameter, a segment (the corresponding power transfer, group delay, or dispersion) can be individually selected. Assuming that (error)k is defined as the desired values(topology) minus the actual values when the result are poorer than the desired value and zero if the actual value is better fitness can be defined as following:

$$Fitness\ is\ sum\ f(x) = [1 + \sum_{i=1}^{n_U} w_U^i \int_{\lambda_{U\ min}^i}^{\lambda_{U\ max}^i} [\max(0, S_U^i(\lambda) - L_U^i(\lambda))]^p d\lambda + \sum_{i=1}^{n_L} w_L^i \int_{\lambda_{L\ min}^i}^{\lambda_{L\ max}^i} [\max(0, L_L^i(\lambda) - S_L^i(\lambda))]^p d\lambda]^{-1} (error)_k$$

Where the symbols are defined as: N_U and N_L are the number of upper and lower limits; w_U^i, w_L^i are the weighting factors for the limits; $\lambda_{U\ min}^i, \lambda_{U\ max}^i, \lambda_{L\ min}^i, \lambda_{L\ max}^i$, are the wavelength ranges for the limits; $L_U^i(\lambda)$ is the definition of the upper limit i ; $L_L^i(\lambda)$ is definition for the lower limit i ; $S_U^i(\lambda)$ is the value of the transfer function, groups delay or dispersion that has to be compared with the upper limit i ; $S_L^i(\lambda)$ is the value of the transfer function, group, delay or dispersion that has to be compared with the lower limit i and p defines the p-norm distance (e.g. $p = 2$). This fitness definition has a lower limit of zero and an upper of one. The weighting factor w_U^i and w_L^i can implement any special behavior without the necessity to modify the fitness calculation procedure. For each candidate circuit (model family), the fitness function of the different models of that circuit are recombined in evaluating the candidate circuit. After a number of

iterations, each candidate circuit has been modeled with all layers levels of resolution. Subsequently, the adjusted fitness of each individual is normalized by the total upper limits and lower limits N_U and N_L members of the population. The filter function in may be shifted along the wavelength axis because a wavelength shift of the final design can be obtained by scaling the geometry. This is common in a real world device tuning element are often implemented to achieve a fine tuning of filter response [26 and 27].

2.9.7.4 MUTATION

The basic idea behind the evolution is to obtain a new chromosome with the optimal fitness value that can be regarded as a search solution. A particular bit is stochastically chosen and its value is flipped to generate new chromosome. This operator randomly changes genes values in the individuals chromosome to some new value contained within the scope of the gene. The probability of changing any particular gene is used set probability of mutation. Until this chromosome is obtained, operations, such as crossover and mutation, are repeatedly executed on the population. At each subsequent generation, a new set of approximations is created by the solution with high fitness. The modification of the geometry is done by using different mutation operators and evaluated them(e.g. mutation operators are the addition and deletion of ring as well as the scaling and displacement of ring elements). The best ones are combined to generate hopefully better ones. Each of them has a probability that can be set individually, some of them with higher values will produce an individual that remnants of past population, and possibly a few randomly generated new individuals. On every mutation evaluation has to be done to assured that the connectivity is maintained and that the constrains like bending radius or the minimum distance between waveguides are fulfilled. The optimizer has access to functional information about the current structure, constraints such as not to separate couplers, not to modify certain types of functional elements, etc. This dat information can be used to optimize the structure without modifying the network topology. A design rule check ensures the correct functionality of the structures. If the optimizer produces a geometrical structure that results from illegal operations, it is rejected, and immediately a new structure will be generated biased toward of the space for which good solutions haave already been seen.

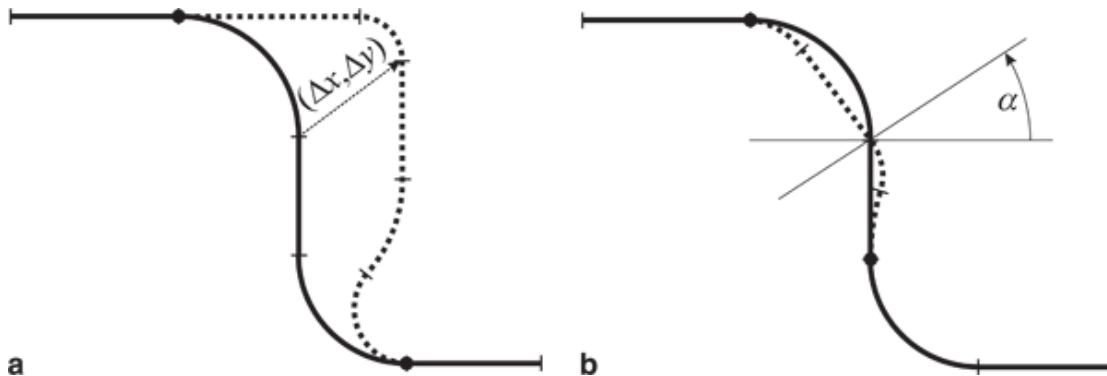


Fig. 2.4.3.4.1 Two mutation operators. (a) node shift, (b) node rotation. The black dots show fix-points that are not moved by the mutation operator. Depending on these statistically chosen fix-points the operation may have different results.

The following section explain the search method for optimization

2.9.7.5 Crossover

Crossover is a method of exchanging gene between two parents(mating) chromosomes in the current population to produce two new offspring(new chromosomes). This new individuals inherits gene value from their parent chromosomes(called elitism). The operation randomly chooses two chromosomes as parents and exchanges parts of them (e.g. combine parent A with genetic information of parent B to produce new offspring). This is done in order to hope that the favorable traits of the parents are passed to new individuals producing better individual. When the number of offspring equals the number in the parents population, the new offspring population is ready to become the new parent population. The original parent is then killed.

2.9.7.6 Evaluation

In order to identify the candidates that may survive to the next generation, each chromosome is evaluated according to the fitness function and assigned a fitness value(a behaviour initially specified by the user).

2.9.7.7 Selection

When the crossover and mutation operations is executing, new chromosomes are generated that may have higher fitness values. However, because the number of chromosomes in a population is fixed during a search, it is necessary to select from among the old and new chromosomes. There are different technique used in selection such as roulette wheel selection [28] and ranking selection. In the early study of Baker's linear ranking algorithm [x] with a selective pressure of 2 is used to ensure that no single individual generate an excessive number of offspring. The fitness of each population can be then define as:

$\hat{F}(x_i) = \frac{2(n_i-1)}{N_{ind}-1}$ were $\hat{F}(x_i)$ is the fitness of the i th individual, n_i the position of the i th individual in the individuals rank, and N_{ind} is the population size. To determine the number of offspring in the roulette wheel selection method each individual is selected as:

$$\text{the expected number of individuals} = \text{integer} \left\{ \left(\frac{\text{FitnessValueofIndividuals}}{\sum \text{FitnessValueofIndividuals}} \right) \times \text{Population size} \right\}$$

Individual fitness values may then be modified to encourage niching behaviour (the formation of sub-populations at different, comparatively optimal, locations) through the use of fitness sharing (Goldberg & Richardson, 1987). Once selection is completed, a new population is ready for the next generation.

In the following fig. 2.4.7.1 illustrate you the cyclus for evolvable harware using mixtrinsic technique.

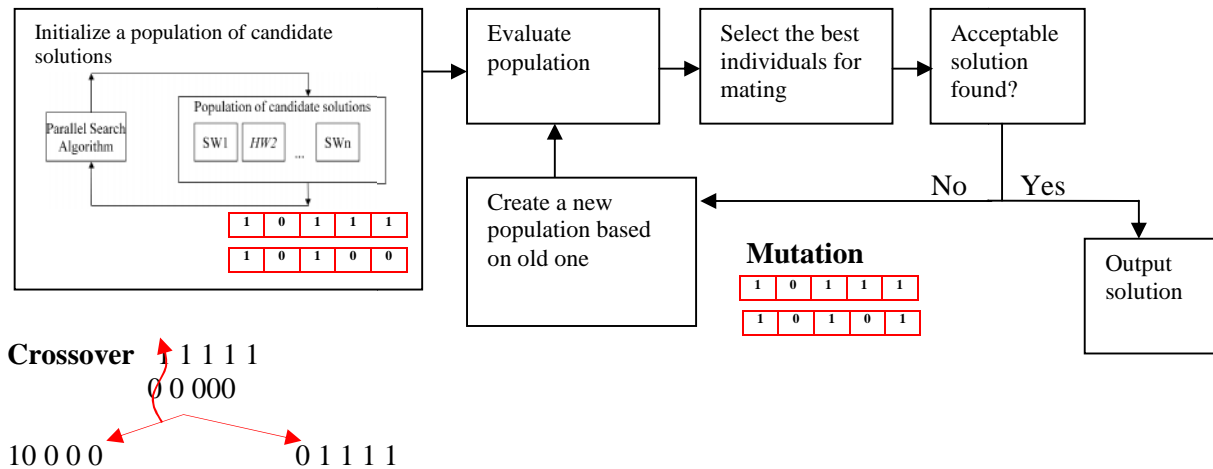


Fig. 2.4.7.1 The evolvable hardware cyclus. Crossover and mutation are two operators used to create beter new population

2.10 Problem formulation

The complexity of circuit connections and encoding chromosomes to evolve the sequential logic circuit may be one of the reasons that not much work has been done in this area. For this experiment some optimization constrains are shown in table 2.5.1 and figure 2.5.1. The initial population size of 20 is chosen from both SW and HW. The chromosomes can be defined as a matrix $[A]_i$ were high and low resolution M1 and m1 is mix with fitness F1 and f1. Mixing SW and HW. The optimization of a circuit topology may be given of N element x and a circuit structure description (e.g node list containing the number of rows and columns). This can represent the total of feasible rings were the total number of visible elements(e.g. rings) is N.

$$X = \{x_1, x_2, \dots, x_n\} \in \mathbb{R}_n \quad (28)$$

Where the parameters of X_n represent the n- dimensional real vector (this is also call the object funtion). Each of the x_n may describe by number of parameters from different layers description(e.g. geometric description, function description, etc.), that are element of a set of population (P). Formaly a P of n individuals could be described as fellow: $P = (c) = (c_1, c_2, \dots, c_{n-1}, c_n)$ where the i^{th} ES-Chromosome c_i is defined as: $c_i = (\text{object-parameters}, \text{strategy parameters})$. This is mixed with the high limits and low limits resolution, M1 and m1 with fitness F1 and f1. The optimization problem can be represent mathematically n as fellow:

$$\begin{array}{ll} \text{Min} & F(s), \quad \mathbb{R} \\ \text{Subject to} & g_j(s) \leq 0 \quad j = 1, 2, \dots, m \\ & s_L^i \leq s^i \leq s_U^i \quad i = 1, 2, \dots, n \end{array}$$

Were s is the solution vector of design variables in the domain \mathbb{R} , $F(s)$ is the objective function to be minimized (or maximized), g_j are the behavioural constrains, the j^{th} inequality constrains function, m the number of inequality constrains, s_L^i and s_U^i are the lower and upper value on transfer functions (bounds) on a typical design s^i , the i^{th} the number of equality constrains.

$$P1 = \{P1, P2, \dots, PL\} \quad (29)$$

The number of parameters L , defines parameter space dimension(the total number of selected parameters e.g. total rings). It has been assumed that each parameter is given by two values: nominal value and design tolerance. Hence, two vectors may be introduced. Vector of elements nominal values \mathbf{NV} .

$$\mathbf{NV} = [NV1, NV2, \dots, NVL] \quad (30)$$

and vector of element tolerances \mathbf{T} .

$$\mathbf{T} = [\text{tol1}, \text{tol2}, \dots, \text{tolL}] \quad (31)$$

In the presented research elements of \mathbf{X} are deletion of ring, the scaling, displacement of ring elements the wavelength ranges, coils, etc. characterized by a single parameters. Then, $L = N$. The circuit topology is described by M design specifications Q_i , that allow for defining an acceptability region in the parameter space.

$$\mathbf{Q} = \{Q1, Q2, \dots, QM\} \quad (32)$$

One specification is considered ($M = 1$), that is a circuit amplitude response deviation from the nominal characteristic

CHAPTER 3: The mixtrinsic evolvable hardware case study (optimization of planar lightwave circuit background of the research project)

The case study has been designed in order to comparable results reported by Erni() and benchmarked the result with avialable comercial tools.

3.1 Evolutionary optimization

Evolutionary optimization use Evolutionary Algorithms (EAs) that mimic biological forces of evolution and self adaptation to solve difficult problem. The procedures are inspired from neo-Darwinian philosophy (theory) which says that stochastic processes such as reproduction and selection, acting on species, are responsible for the present life forms we know. In simple terms natural evolution describes how a population of individuals strives for survival. During reproduction genetic material from each parent creates an offspring. Each individual has an associated fitness that ultimately determines the survival probability. Highly fit individuals have a high probability of surviving to reproduce in future generations.

The mean proposed behind the EAs is that each individual is a unique solution to the optimization problem of interest. Each solution is referred to as an individual and the set itself is referred to as the population. New individuals are created by varing individuals in the current population randomly each generation. Each individual in the population is often called chromosome or genotype. The success of the optimization problem depends on the representation diverse operation such as the chromosomes, fitness function, method of crossover, mutation operation and different information from the chromosome. While the mutation adds new information to a chromosome, it also destroy useful information held in the chromosome with illusion to create better generations (offsprings). The offspring would then replace its parent in the next generation, if it had a better fitness (Back and Schwefel, 1993). Every individual is evaluated and the best individuals are selected for the next population. For reasonable performance of the optimization procedure, it is necessary that these individuals be scattered through the entire solution space. Once it initialized, every individual is evaluated using the function $f(x)$. The value thus returned from the function is referred to as the *fitness* value of the individual. After evaluation, the individuals with the lowest fitness values are selected to form the next generation of individuals and the remaining are discarded. This process is then repeated until a stopping criterion is achieved. This could either be a fixed number of generations or a minimum value of the fitness function.

3.2 THE CMA EVOLUTION STRATEGY

Evolutionary algorithms (EAs) such as evolutionary strategy and coveriance matrix adaptation (CMA-ES) is a state-of-the-art heuristic optimization algorithm (Hansen and Ostermeier 1997, 2001). CMA-ES stands for stands for Covariance Matrix Adaptation Evolution Strategy. CMA-ES can be described as a randomized balck blox search algorithms and the flow chart of this method is illustrated in Fig. 3.2.1. It's an (search)algorithm for dificult non-linear non convex optimization problems in continious domain. The CMA-ES is avariable metric algorithms which efficiently its search distribution based to the problem at the hand. Typically the CMA-ES is applied to unconstrained or bounded constraint optimization problems, and this with the fact that it scan be used with small population sizes, is the reason why CMA-ES has high efficency in his implementation.

The key idea of CMA-ES algorithms is to alter the mutation distribution such that the probability to reproduce steps in the search space that led to the actual population (i.e., produced offspring that were selected) is increased. This enables the algorithm to detect correlations between object variables and to become invariant under affine transformations of the search space. This elaborated evolutionary algorithm (CMA-ES) makes maximum use of the information contained in the search history for self-adaptation of the search direction which is defined in terms of the covariance matrix of a normal distribution from which new tentative solutions or, in the language of evolutionary algorithms, new individuals are drawn. Thereby

the population size in the evolutionary strategy is decoupled from the dimension of the search space. This means that a drawback of stochastic search, the need for evaluation of a large number of possible solutions, is alleviated. The algorithms implement several important concepts for adapting search distributions. The first one is known as *derandomization* meaning that the mutation distribution is adapted in a deterministic way. The second principle is *cumulation*, which refers to taking the search path of the population over the past generations into account, where the influence of previous steps decays exponentially.

Each individual represent an n -dimensional real valued object variable vector. It is solely based on the ranking of candidate solutions and therefore invariant under order-preserving transformations of the objective function. The CMA-ES is invariant under angle-preserving transformations of the input space, like translation, rotation and reflection, given that the initial solution is transformed accordingly. The algorithm is not affected by an overall rescaling of the search space, given that the initial scaling parameter is chosen accordingly. The evolution is done by using the operators recombination and mutation. The core idea of CMA-ES algorithms is to alter the Mutation is realized by adding a normally distributed random vector with zero mean, where the completed covariance matrix adapted during evolution to improve the search strategy. More formally, the objective parameters $x_k^{(g+1)}$ of offspring $k = 1, \dots, \mu$ created in generation g are given by: $x_k^{(g+1)} = \bar{x}^{(g)} + N_k^{(g)}(0, \sigma^{(g)^2} C^{(g)})$,

where, $\bar{x}^{(g)}$ denotes the center of mass of the population in the next generation g and $N_k^{(g)}(0, \sigma^{(g)^2} C^{(g)})$ Are independent realizations of an n -dimensional normally distributed realization random vector with zero mean and covariance matrix $\sigma^{(g)^2} C^{(g)}$. The strategy parameters, both the matrix $C^{(g)}$ and so called global step-size $\sigma^{(g)}$, are updated online using the covariance matrix adaptation (CMA) method. In our implementation, we ensure that $\sigma^{(g)} \cdot \lambda_{min}^{(g)} \geq \sigma_{min}$, where $\lambda_{min}^{(g)}$ is the smallest eigenvalue of $C^{(g)}$ (i.e. a minimum variance of the shortest principal axis of the mutation ellipsoid can be guaranteed). The algorithm in CMA-ES recombination based selection is used (i.e., the μ best of the offspring from the next parent population. The population sizes are chosen according to the heuristic $\lambda = 4 + [3 \ln n]$ and $\mu = [\lambda/4]$ shown by Hansen and Ostermeier(2001).

Each individual in the population $P = \{ \vec{\alpha}_1, \vec{\alpha}_2, \dots, \vec{\alpha}_\mu \}$ referred to by an index $k = 1, \dots, \mu$ has a phenotype $\alpha_k = \begin{pmatrix} \vec{x}_k \\ \vec{z}_k \end{pmatrix}$ with $\alpha_k \in \mathbb{R}^n$, where \vec{x}_k is the standard ES parameter vector and \vec{z}_k is the associated standard deviation vector. Three matrices are needed for the algorithms: the covariance matrix $C \in \mathbb{R}^{n \times n}$, the eigenvector matrix of C named $B \in \mathbb{R}^{n \times n}$ and the diagonal matrix of the square rooted eigenvalues of C named $D \in \mathbb{R}^{n \times n}$. The μ individuals of the initial population are randomly defined (are randomly chosen within the domain boundaries of f and are set to the null vector). Matrix B is set to the identity matrix, the diagonal matrix D is set to represent the domain boundaries $D_{ii} = H_i - L_i, \forall i = 1, \dots, n$. C is calculated as the product of BD and its transpose: $C = BD(BD)^T$.

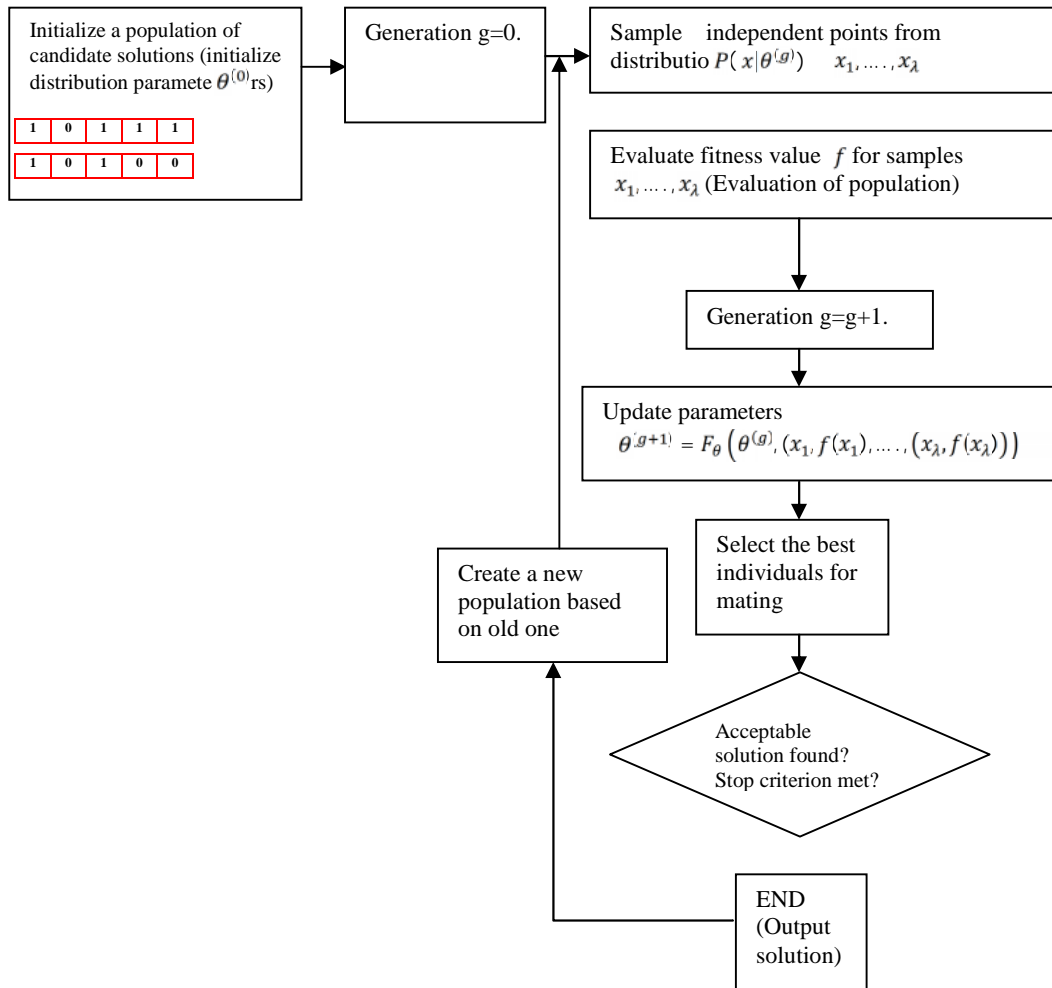


Fig. 3.2.1 The CMA-ES flow chart. Crossover and mutation are two operators used to create beter new population

3.2.1 Recombination

Using the global weighted intermediate recombination method in conjunction with a sorted population (the best individual is number 1, the worst is μ), identical children are created with a phenotype:

$$(\vec{X}_h)_i = \sum_{k=1}^{\mu} \omega_k \cdot (\vec{X}_k)_i, \quad i = 1, \dots, n \quad (4)$$

$$(\vec{Z}_h)_i = 0, \quad i = 1, \dots, n \quad (5)$$

in which the individual index h goes from $(\mu+1)$ to $(\mu+)$ and ω_k are the weights of the recombination, which are themselves parameters of the algorithm. In this study we take

$(\omega_k) = (\log(\mu + 1) - \log(k)) / \sum_{l=1}^{\mu} (\log(\mu + 1) - \log(l))$ which gives more weight to the best individuals population.

3.2.2 Mutation

The main mechanism of the implemented operator is changing the allele values by adding random noise drawn from a normal distribution. The randomness from the normal distribution is stored in the individual phenotype and used in the adaptation phase. The mutation acts on each of the children with a modification of their phenotype in the following order:

$$\begin{aligned} (\bar{z}_h)_i &\leftarrow N_i^h(0, 1), \quad \forall i = 1, \dots, n \\ (\bar{x}_h)_i &\leftarrow (\bar{x}_h)_i + \sigma_F \cdot \sum_{k=1}^n B_{ik} \cdot D_{kk} \cdot (\bar{z}_h)_k, \quad \forall i = 1, \dots, n, \end{aligned} \quad (6)$$

where $N_i^h(0, 1)$ is a random number drawn from a normal distribution sampled anew for each element i of each individual $h=(\mu+1), \dots, (\mu+)$ and the symbol \leftarrow means that $(\bar{z}_h)_i$ and $(\bar{x}_h)_i$ will take the values on their RHS. The global step size $\sigma_F \in \mathbb{R}_+$ is a (problem-dependant) parameter of the algorithm.

3.2.3 Selection

Elitist selection is used to retain the μ best individuals of the children.

3.2.4 Adaptation

The global step size $\sigma_F \in \mathbb{R}_+$ is adapted using a ‘‘conjugate’’ evolution path $\bar{s} \in \mathbb{R}^n$, realised in the following order:

$$\begin{aligned} \bar{s} &\leftarrow (1 - c_s)\bar{s} + \sqrt{\mu_{eff} \cdot c_s(2 - c_s)} \cdot B \cdot \sum_{k=1}^{\mu} \omega_k \bar{z}_k \\ \sigma_F &\leftarrow \sigma_F \cdot \exp\left(\left(\frac{s}{\bar{\chi}_n} - 1\right) \cdot \frac{c_s}{d_s}\right), \end{aligned} \quad (7)$$

where $\bar{\chi}_n = \sqrt{n(1 - 1/4n + 1/21n^2)}$, $c_s = (\mu_{eff} + 2)/(n + \mu_{eff} + 3)$,

$d_s = 1 + 2 \cdot \max(0, \sqrt{(\mu_{eff} - 1)/(n + 1)} - 1) + c_s$, $\mu_{eff} = 1 / \sum_{k=1}^{\mu} \omega_k^2$ and s is the vector norm of \bar{s} . The initial conjugate evolution path is $\bar{s} = \bar{0}$.

The covariance matrix $C \in \mathbb{R}^{n \times n}$ is adapted using the evolution path $\bar{c} \in \mathbb{R}^n$ in the following way:

(8)

$$\vec{c} \leftarrow (1 - c_c)\vec{c} + H_s \cdot \sqrt{\mu_{eff} \cdot c_c(2 - c_c)} \cdot BD \cdot \sum_{k=1}^{\mu} \omega_k \vec{z}_k$$

$$C \leftarrow (1 - c_{cov})C + c_{cov} \cdot \frac{1}{\mu_{eff}} \cdot \vec{c} \cdot \vec{c}^T + c_{cov} \cdot \left(1 - \frac{1}{\mu_{eff}}\right) \cdot$$

$$\sum_{k=1}^{\mu} (BD \cdot \vec{z}_k)(BD \cdot \vec{z}_k)^T$$

where

$$c_{cov} = 1/\mu_{eff} \cdot 2/(n + \sqrt{2})^2 + (1 - (1/\mu_{eff})) \cdot \min(1, (2\mu_{eff} - 1)/((n + 2)^2 + \mu_{eff})),$$

$c_c = 4/(n+4)$, $H_s = 1$ if $s/\sqrt{1 - (1 - c_s)^{2(g+1)}} < (1.5 + (1/(n - 0.5)))\bar{\chi}_n$ or 0 otherwise (the symbol g corresponds to the generation number). The initial evolution path is $\vec{c} = \vec{0}$.

Once adapted, the orthogonal matrix B and diagonal matrix D are obtained through principal component analysis of C (i.e. $C = BD^2B^T$).

The filter structure to be treated is a double-ring resonator (DDR or multiple rings resonator). It consist of two different radii r_1 and r_2 located between the input and output waveguides (see Fig. 3.1). This structure increase the fitness. The waveguides are coupled by three directional couplers with amplitude coupling ratios of K_1 , K_2 and K_3 . The spacing between the waveguides has the most impact on the coupling coefficient[xyz] Each ring has a different resonance wavelength. By choosing a specific ratio between the two radii r_1 and r_2 it is possible to obtain a free spectral range related to the least common multiple of the two resonance wavelengths. The quality of the resonator can be measured by several propertied such as: the free-spectral range(the spacing between adjacent reconances), the quality factor (a measurement of the effectiveness in the storing energy), the fitness (the ratioof the FSRto the with of the resonance and the extinction ratio (the ratio of the transmission at resonance to the offresonance transmission) .

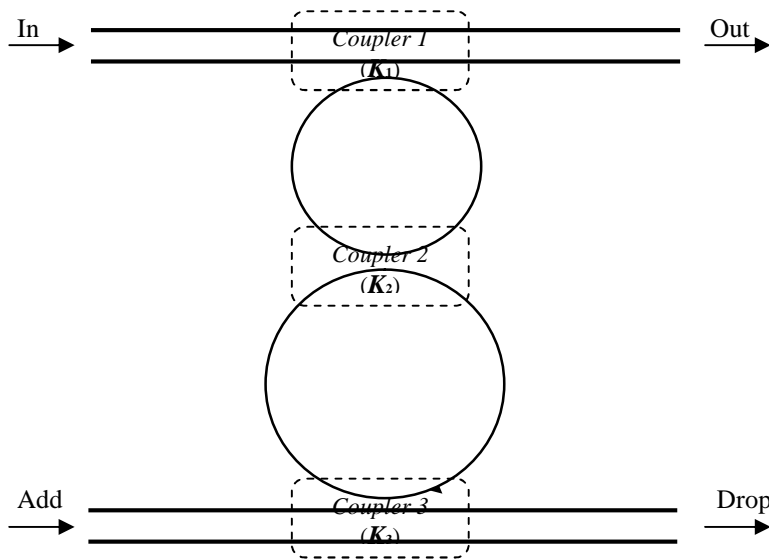


Fig.3.1 Schematic diagram DDR filter structure (Oda et. al. 1991).

The defined constraints is not to separate the couplers, not to modify certain type of functional elements(e.g. coupling coefficient and delay line lengths). Optimizae the structure without modefying the network topology. Driven by mixtrinsic evolution is driven genetic algorithms(GA), genetic programming (GP) or evolution strategies (ES). We choose the ES approach which is first introduce by Ingo Rechenberg(1963, 1973) and Hans Paul Schwefel at the Technical University of Berlin(1965, 1977), using normally distributed mutation to modify real-valued vectors. the problem is represented in a chromosome, also called genome (sequence of genes). The genome consists of a gene string. The position of a gene in a chromosome is called locus. Each of the genes represents a dimension in the problem space.

Every inverse problem consist of two main parts the forwardsolver and the strategy to optimize the result. The particular implemtation of that it operates on tree representation levels. Combining this with mixtrinsic EHW that operates on two representaion levels. Each of this representaions have different level of abstraction this enable the optimizer to use data that would not be available in standard implemetaion.

For the topology structure an evolution quality figure can be used to represent the capability of the population to produce further more successful structures when continue the optimization would be usefull. Such figure may be defined using a number of sub-populations together with fitness of the best representing of each sub-population, normalized using the temporal maximum fitness in the whole

population. The equation can be written as follow: $C_p(n) = \frac{1}{\hat{F}_n} \sum_{i=1}^{N^{SP}(n)} \hat{F}_i^{SP}(n)$

where $C_p(n)$ is the evolution quality figure after n optimization steps, \hat{F}_n is the temporal maximum fitness, $N^{SP}(n)$ the number of sub-population and $\hat{F}_i^{SP}(n)$ is the fitness of most sucessfull representantod the i^{th} sub-population.

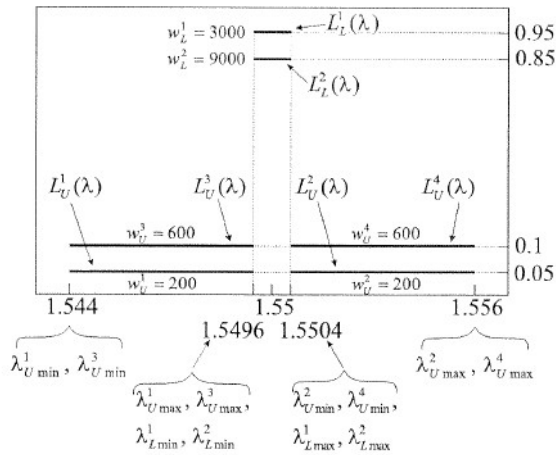


Figure 3.1. The optimization constrains are illustrated in the figure here above each of them have their own weight factor bened the line.

CHAPTER 4: The Experimental Design and Results

The experiment has been divided in 3 phases. The first phase consists in test if CMA-ES algorithm is capable to do the job as optimization engine for EHW. The result will be compared with commercial tools for optimization of planar lightwave circuit. Analyse the utility of CMA-ES in optimizing the topology of planar lightwave circuit. The second phase consists into incorporate forward solver with CMA-ES for the optimization part. The last phase consist into incorporate the mixtrinsic evolution method with the forward solver, including having CMA-ES for the evolutionary algorithm part.

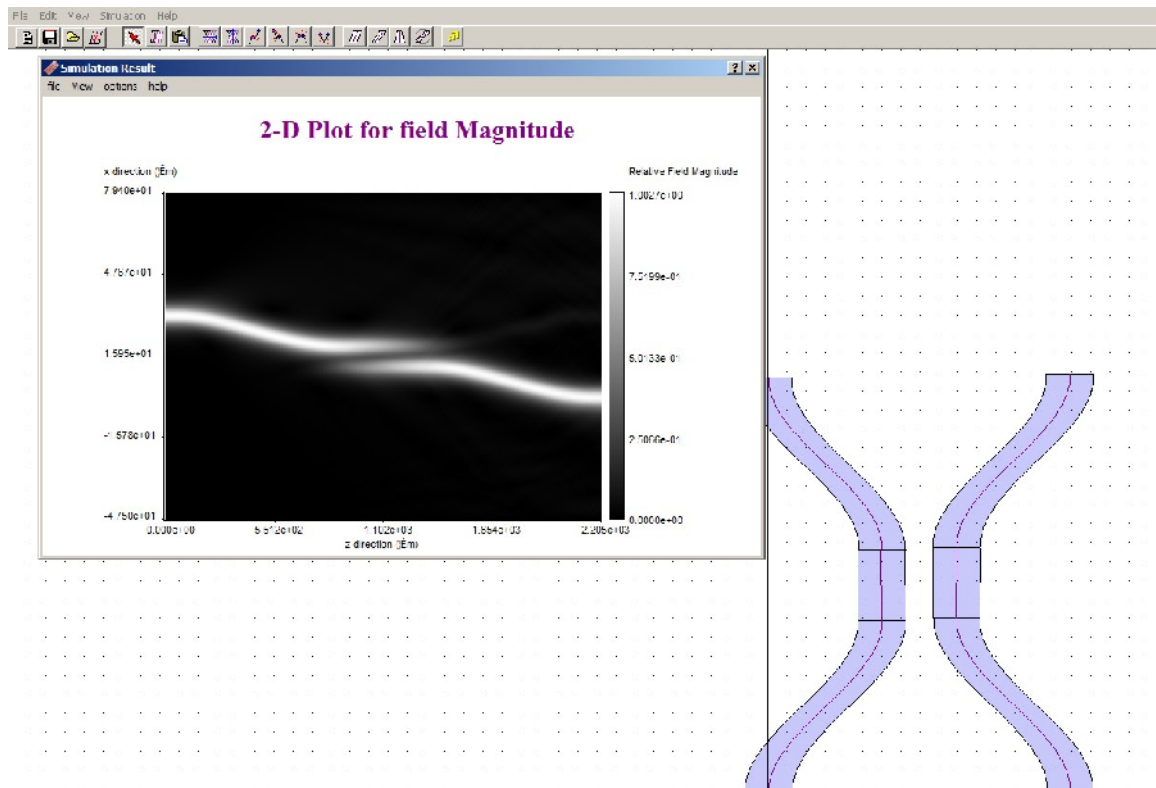
4.1 ION_CAD

The initial population of six chromosomes each having 5 variables has been generate from the ION-CAD tool.

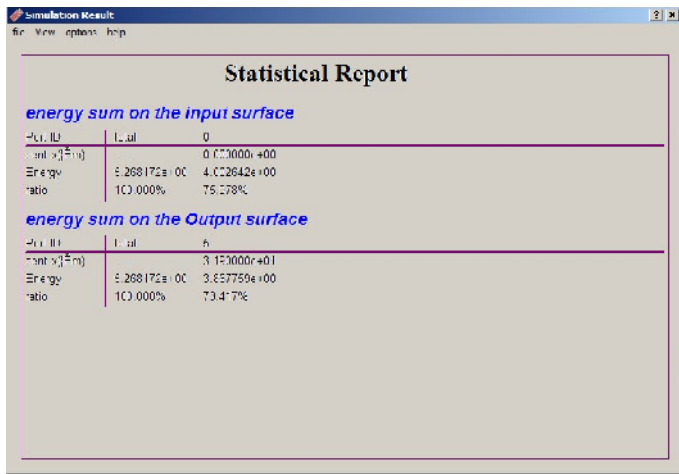
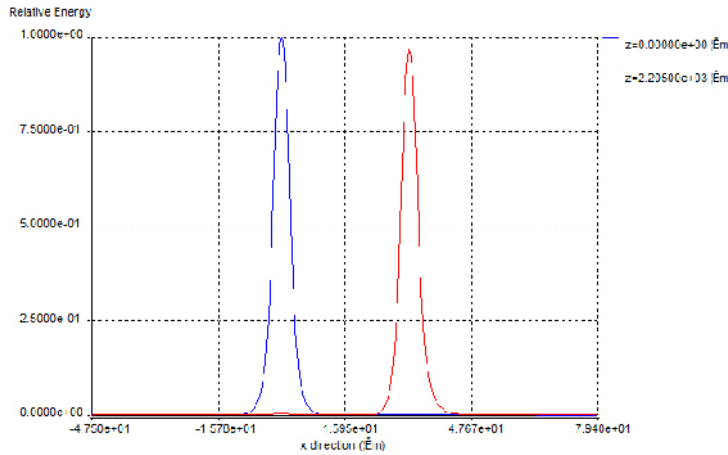
$$pop = \begin{bmatrix} 0 & 0 & 12 & 910 & 5 \\ 31,8 & 10 & 19,8 & 920 & 5 \\ 12 & 910 & 12 & 1280 & 5 \\ 19,8 & 920 & 19,8 & 1290 & 5 \\ 12 & 1280 & -3,55 & 2190 & 5 \\ 19,9 & 1295 & 31,9 & 2205 & 5 \end{bmatrix}$$

The constrains from the upper limit and the lower limit are giving as fellow

The result using EHW the intresicly with refractive indices of the waveguide and the cladding layer are n_w 1.465 and $n_c = 1.46$ respectively. The waveguide width $W=5 \mu\text{m}$, the gap between the two waveguides is $G=3\mu\text{m}$. S bend is used as the input and output waveguides.



1-D Plot for field Magnitude



4.2 CMA-ES results

The aim is to optimize the topology of an integrated planar lightwave circuit, we want to optimize the coupling length to realize the maximal output from waveguide at λ and in our test case optimal means similarity to reference topology. In order to make those lightwave circuits some basic blocks need to be built which are shown in paragraph 2.9.2. These building blocks need to be as computing units taking input1 and input2 as input signals and which returns output1 and output 2. Each of these building blocks has some parameters X_1, Y_1, X_2, Y_2 , etc. So in the end, we can couple a number of those building blocks in a circuit by specifying the parameters of the building blocks. The CMA-ES adapts the step size, a scaling parameter that tunes the granularity of the search, by comparing the actual topology design to that of the building blocks with a random walk. CMA-ES proposes robust default parameters: the population size is set to $4 + 3 \log(n)$ and the initial step-size to a third of the parameters range.

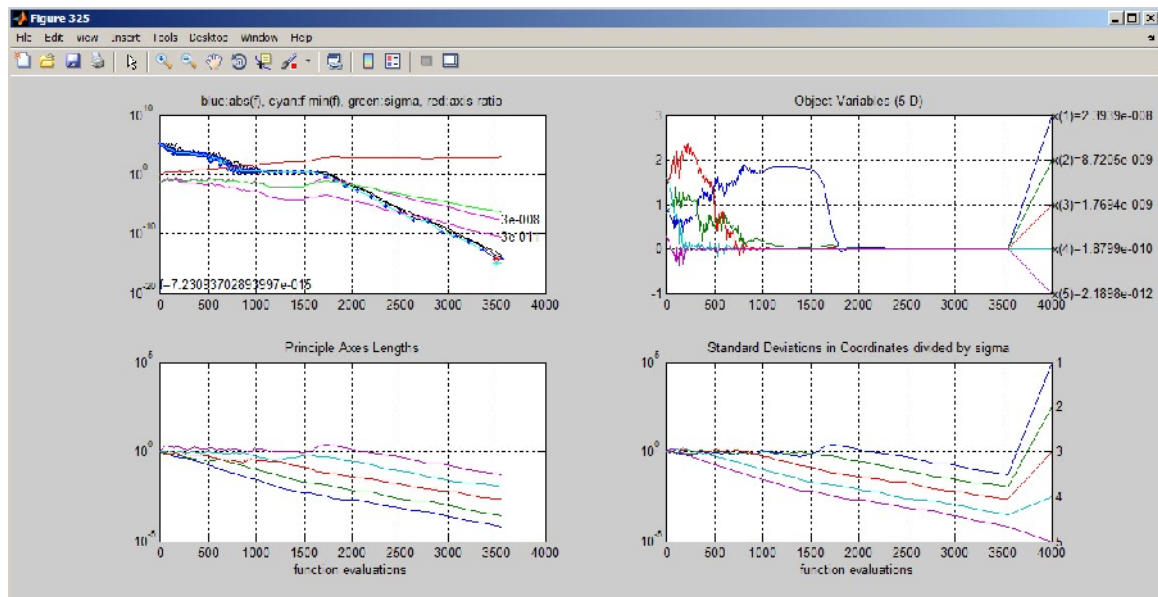


Figure 4.2.1

CHAPTER 5: Conclusions

5.1 The limitations of the CMA-ES

The restrictions of the CMA-ES carried out for the test case in optimize the topology of an integrated planar lightwave circuit relies on neighborhood. When the neighborhood information is useless, CMA-ES perform poorly. The major design criterion for the CMA-ES is the invariance properties (for example, a class of optimization object functions might share a common coordinate system that is optimal for solving all instances. In such case, algorithms that a priori utilize the distinguished coordinate system are potentially better than a coordinate system invariant algorithm.

5.2 The strengths of the CMA-ES

CMA-ES can be outperformed on separable problems, where the given coordinate system is highly distinguished. Similarly, it can be beneficial to sacrifice invariance under order preserving transformation of the function value (which is due to the rank-based selection in Evolutionary strategy). For example, on *noise-free* quadratic functions, quasi-Newton methods are typically an order of magnitude faster than CMA-ES, because they exploit the function *values* explicitly.

The strengths of the implemented CMA-ES as evolutionary algorithm prove to be very accurate and fast for practical resonator filter structure and topology optimization of an integrated planar lightwave circuit. It is possible to switch between the three representation levels and therefore, to extract any information needed. Since each representation level is available as an ASCII text, the user can easily supervise the steps and interact at different levels. The use of the scattering matrices for analysis of integrated waveguide structures reduces the complexity of the calculations while only degrading the obtained results very slightly. In this implantation, all waveguides are assumed to be single-mode.

5.3 Future work

Additional work has to be done to enable the system to autonomously discover new filter topologies. Such a functionality could be implemented by acquiring statistical information during the optimization and using a database of well performing structures. The statistical information could partially replace the crossover operator. A structure database may be used to compose filters out of more complex functional blocks. It is nevertheless not yet clear, how the optimization would function in the future. The rapid development of the computer performance will certainly allow "inventor" software to become a reality.

5.4 Concluding remarks

A procedure was implemented for the topological optimization of planar lightwave circuits. It is very flexible and allows the optimization of many aspects of the structure. Especially it is possible to optimize the filter characteristics and the corresponding dispersion at the same time.

Since the phase conditions are very critical to filter characteristics, two almost identical structures may have completely different performance. Therefore, finding a good topology by just randomly putting together basic waveguide elements are very unlikely. Given a topology that corresponds to the desired structure, the optimizer is then able to find an optimal configuration. A given topology defines the number and types of directional couplers, as well as the feed-backs. If an optimal structure cannot be found using the given topology the optimizer can modify the functional structure to obtain a new topology.

The challenge of conventional design is replaced with that of designing an evolutionary process that automatically performs the design in our place. *This may be harder than doing the design directly*, but makes autonomy possible.

Recommended literature

- [1] D.Ioan, G.Ciuprina, reduced order models of on-chip passive components and interconnects, Workbench and test structures, in Scientific Computing in Electrical Engineering
- [2] R. S. Zebulum, M. A. Pacheco, M. Vellasco, Evolvable systems in hardware design: taxonomy, survey and applications, International Conference on Evolvable Systems: From Biology to Hardware (ICES 96)
- [2] E.Vergison, "A Quality-Assurance guide for evaluation of mathematical models used to calculate Major Hazards" Brussels, Belgium: Solvay S.A., Rue de Ransbeek, 20 November 1995.
- [3] Spühler, M.M., D. Erni and J. Fröhlich. Opt. and Quantum Electron. 30 305, 1998b.
Spühler, M.M., D. Wiesmann, P. Freuler and M. Diergardt. Opt. and Quantum Electron. 31 751, 1999.
- [4] Erni, D., M.M. Spühler and J. Fröhlich. Opt. and Quantum Electron. 30 287, 1998.
- [5] Wiesmann, D., D. Erni, J. Fröhlich, H. Rothuizen, R. Germann, G.-L. Bona, C. David and H. Jäckel. Apodization of a Grating Filter by Concatenation of Bragg Gratings with Different Ridge Patterns. In Proc. ECIO'99, 159-162, 1999.
- [6] Y.M. Xie, G.P. Steven, A simple evolutionary procedure for structural optimization, Comput. Struct. 49 (1993) 885–896.
- [7] P.Tanskanen, The evolutionary structural optimization method: theoretical aspects, Comput. Methods Appl. Mech. Engrg. 191 (2002) 5485–5498
- [8] R. Fournier, Practical Guide to Structured System Development and Maintenance, Prentice-Hall, Englewood Cliffs, NJ, 1991, Chapter 13, pp. 316–322.
- [9] J.R. Koza, F.H. Bennett III, D. Andre, and M.A. Keane, Genetic Programming III, Darwinian Invention and Problem Solving, Morgan Kaufmann Publishers
- [10] A. Stoica, C. Salazar-Lazaro, D. Keymeulen, and K. Hayworth. Evolution of CMOS circuits in simulations and directly in hardware on a programmable chip. In W. Banzhaf, J. Daida, A. E. Eiben, M. H. Garzon, V. Honavar, M. Jakiela, and R. E. Smith, eds., Proc. of the Genetic and Evolutionary Computation Conference, Orlando, FL, pp. 1198–1203, San Francisco, CA, 1999. Morgan Kaufmann Publishers.
- [11] Stoica, A., Keymeulen, D., Arslan, T., Duong, V., Zebulum, R., Ferguson I., Guo, X.: Circuit Self-Recovery Experiments in Extreme Environments. In: EH'04: Proc. of the 2004 NASA/DoD Workshop on Evolvable Hardware, ed by Zebulum, R. et al., Seattle USA, 2004 (IEEE Computer Society, Los Alamitos 2004) pp 142-145
- [12] Koza J. R., Andre D., Bennett III F. H., and Keane M. A., (April 1997) Design of a High-Gain Operational Amplifier and Other circuits by Means of Genetic Programming, in Proceedings of the 6th International Conference on Evolutionary Programming (EP97), now published in Lecture Notes in Computer Science, Vol. 1213, pages 125-135, 1997.
- [13] P. Chongstitvatana and C. Apornthewan, "Improving correctness of finite-state machine synthesis from multiple partial input/output sequences," in Proceedings of the 1st NASA/DoD Workshop of Evolvable Hardware, 1999, pp. 262–266.
- [14] S. Louis, "Genetic algorithm as computational tool for design," PhD Dissertation, Department of Computer Science, Indiana University, 1993.
- [15] H. Hemmi, J. Mizoguchi, and K. Shimohara, "Development and evolution of hardware behaviours," Brooks and Maes (eds.), Artificial Life IV, Proc. 4th Int. Workshop Synthesis Simulation Living Syst., R. Brooks and P. Maes, Eds. Cambridge, MA: MIT Press, 1994, pp. 371–376.
- [16] R.A. Rutenbar, G.E. Gielen, and B.A. Antao, eds., Computer-Aided Design of Analog Integrated Circuits and Systems, IEEE Press, Piscataway, 2002

- [17] Thomas Beack, Adaptive business intelligence based on evolution strategies: some application examples of self-adaptive software, Elsevier Science Inc, 2002
- [18] März, R. Integrated Optics, Design and Modeling. Artech House, Inc., Norwood, MA, 1995, 336 p.
- [19] Oppenheim, A.V. and R.W. Schaffer. Discrete-Time Signal Processing. 879 p. International Edition, Prentice-Hall, Englewood Cliffs, NJ, 1989.
- [20] Jinguji, K. J. Lightwave Technol. 14 1882, 1996.
- [21] Dragone, C. J. Lightwave Technol. 7 479, 1989.
- [22] Kuznetsov, M. J. Lightwave Technol. 12 226, 1994.
- [23] Orta, R., P. Savi, R. Tascone and D. Trincherio. IEEE Photon. Technol. Lett. 7 1447, 1995.
- [24] T. Kalganvoa and J. Miller, "Circuit layout evolution: an evolvable hardware approach," Colloquium on "Evolutionary hardware systems," IEE Colloquium Digest: London, UK, 1999.
- [25] Spühler, M.M., D. Erni, toward structural optimization of planar integration lightwave circuits, Opt. and Quantum Electron. 32 701-718, 2000.
- [26]
- [27]
- [28] Shackleton M and Marrow P (Eds): 'Nature-inspired computation', Special Issue of BT Technol J, 18, No 4, (October 2000).
- [29] J.M. Wojciechowski, L.J. Opalski, and K. Zamly ski, "Design centring using an approximation to the constraint region", IEEE Transactions on Circuits and Systems – I: Regular Papers. 5 (3), 598–607 (2004).
- [29] H. Tian and L. Milor, "Yield optimisation for integrated circuits", ISR TR 92-103, <http://hdl.handle.net/1903/5284> (1992).
- [30] L. Zielinski and J. Rutkowski, "Design tolerancing with utilization of gene expression programming and genetic algorithm", Int. Conf. Signals and Electronic Systems ICSES, 13-15 (2004).
- [31] T. Bäck, D.B. Fogel, and Z. Michalewicz, Evolutionary Computation I – Basic Algorithms and Operators, IOP Publishing Ltd, Bristol, 2000.
- [32] T. Bäck, D.B. Fogel, and Z. Michalewicz, Evolutionary Computation II – Advanced Algorithms and Operators, IOP Publishing Ltd, Bristol, 2000.
- Hitoshi Hemmi Jun_ichi Mizoguchi and Katsunori Shimohara_ Development and Evolution of Hardware Behaviors_ Arti_cial Life IV Proceedings of the fourth international workshop on the synthesis and simulation of living systems
- Hitoshi Hemmi Jun_ichi Mizoguchi and Katsunori Shimohara_ Development and Evolution of Hardware Behaviors_ Toward Evolvable Hardware The Evolutionary Engineering Approach_ Lecture Notes in Computer Science
- Others
- Horgan, G. (2000) Construction of a Quality Assurance and Measurement Framework for Software Project, PhD Thesis, Kingston University, UK.
- Khoshgoftaar, T. M., and Allen, E. B. 2000. A practical classification rule for software quality models. IEEE Transactions on Reliability 49(2): 209-216.
- D.Ioan, M.Radulescu,G.Ciuprina, Fast Extraction of Static Electric Parameters with Accuracy Control, in Scientific Computing in Electrical Engineering (W.H.A. Schilders et al Eds), Springer, 2004,pp.248-256.
- Thomas Bäck and H.P Schwefel, An overview of Evolutionary Algorithms for parameters optimization. Evolution Computation, 1(1):1-23, 1993 A classical paper(with fromalistic algorithm decriptions) that „unified“ the field

A. Thompson, "Evolving electronic robot controllers that exploit hardware resources," in Proceeding 3rd European Conference on Artificial Life (ECAL 95) A Moreno, J. J. Merelo, and P. Chacon (eds.), Springer-Verlag, vol. 929, 1995, pp. 640–656.

McEachern, L. (1999), "Constrained Circuit Optimization Via Library Table Genetic Algorithms", 0-7803-5471 -0/99 IEEE.

Barbarossa, G., A.M. Matteo and M.N. Armenise. J. Lightwave Technol. 13 148, 1995a.

Barbarossa, G., A.M. Matteo and M.N. Armenise. Compound Triple-Coupler Ring Resonators for Selective Filtering Applications in Optical FDM Transmission Systems. In Proc. SPIE, 2401 86±94, 1995b.

Chu, S.T., W. Pan, S. Sato, T. Kaneko, B.E. Little and Y. Kokubun. IEEE Photon. Technol. Lett. 11 688, 1999.

Madsen, C.K. and G. Lenz. IEEE Photon. Technol. Lett. 10 994, 1998.

Marcuse, D. Theory of Dielectric Optical Waveguides. Academic Press, Inc., San Diego, CA, 1991, 380 p.

Yao, X. and T. Higuchi. 1999. "Promises and challenges of evolvable hardware", *IEEE Trans. Systems, Man, and Cybernetics, C* 29(1), 87-97.

SpuÈ hler, M.M., D. Wiesmann, P. Freuler and M. Diergardt. Opt. and Quantum Electron. 31 751, 1999.

The following illustration shows the evolvable EA's process.

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