Sensitivity analysis of on-chip passive integrated structures to environmental variation using parametric compact models

Jagoda Plata, Michal Dobrzynski and Sebastian Gim
Numerical Methods Laboratory, Faculty of Electrical Engineering, "Politehnica" University of Bucharest,
Spl. Independentei 313, 060042 Bucharest, Romania
plata@lmn.pub.ro, d_michal@lmn.pub.ro, seb@lmn.pub.ro

Abstract — The integration of analog and digital sub-systems on a single die necessitates the use of highly accurate but compact models of electromagnetic effects in integrated passive structures for the successful design of next generation Integrated Circuits (IC). This paper examines the use of the Adjoint Field Technique (AFT) and the Finite Integral Technique (FIT) to extract parametric compact models of integrated passive structures. A software prototype implementing these methods is then used to investigate the sensitivity of several standard benchmark structures to environmental variations.

I. Introduction

Driven by consumer demand, the trend in today's semiconductor industry is not only towards more compact integrated circuits (IC) [1], but also more complex functionality. This leads to the integration of analog (RF) and digital sub-systems on a single silicon chip. Furthermore, due to greater demand for bandwidth by multimedia applications, the operating frequency of these integrated circuits is also increasing. At gigahertz frequency of operation however, electromagnetic (EM) signal propagation on interconnect structures are very susceptible to changes in the properties of the environment.

Because of this, accurate parametric compact models are needed for the successful design of next generation integrated mixed signal silicon. The CHAMELEON-RF (CHRF) project was initiated to develop tools and methodologies for comprehensive high accuracy modelling of on-chip electromagnetic effects considering environmental variability [5]. The CHRF software prototype enables the extraction of parametric compact models (SPICE compliant) of passive integrated structures for sensitivity analysis of material variation in the environment. Furthermore parametric models enable the simulation of sensitivity to variation without recomputing new models for the whole design.

In this paper, we first present in section 2, the keypoints of parametric model extraction using the Adjoint Field Technique (AFT) from dual Finite Integration Technique (dFIT) solvers [6]. Section 3 then presents results from sensitivity analysis of several standard benchmark structures using the CHRF software prototype.

II. Extraction Methods

Parametric compact modeling of EM effects in integrated on-chip passive structures can be obtained using the AFT and Taylor Series (TS) expansion [3]. In numerical analysis of fields in the time domain we use dFIT [4] for discretization of the continuous model. As a result, sparse state-space representation of the component is obtained, which is further approximated using post processing Model Order Reduction (MOR) techniques [2]. From this, a dimensionally- and materially- parametrized model is obtained that enables the computationally efficient simulation of on-chip integrated passive structures.

III. Results of Benchmark Validation

The described modeling methods were validated by comparing simulation results with measured data for fabricated benchmarks. These structures include basic structures like coupling from device to device and substrate coupling, but also several commonly used RF blocks.

The Chamy prototype code developed by Numerical Methods Laboratory (LMN) within the CHRF project was then used to simulate and validate several benchmark structures. Finally, sensitivity analysis of environmental variation on selected test structures was performed. The parameter sensitivity accuracy method was estimated with comprehensive test Chamy TS vs. Chamy full block analyze.

All validated mathematical models were developed in LMN as fully parametrized blocks based on real elements values.

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V. References

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